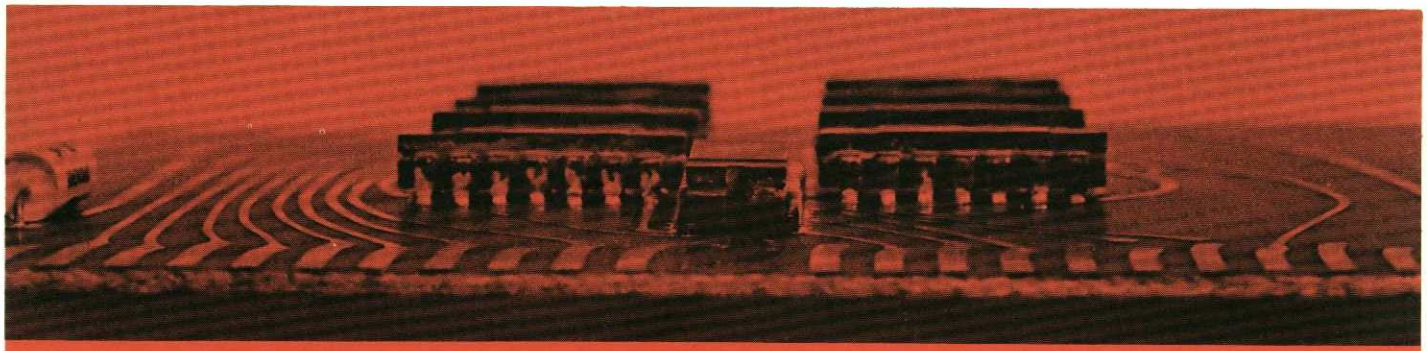
SDS

Scientific Data Systems



IC DIGITAL LOGIC MODULES

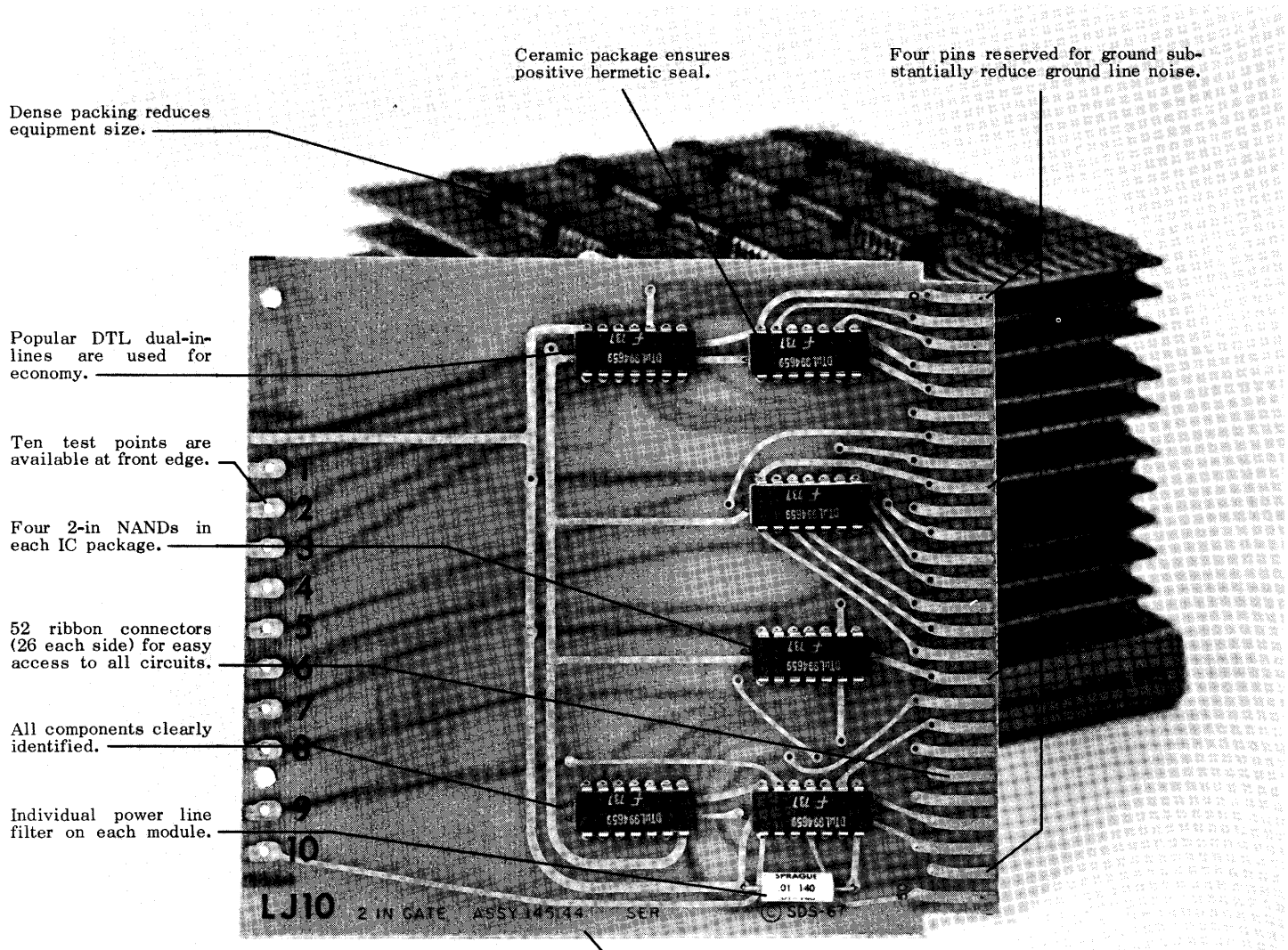
J Series

Revision 1
December 1968

SDS J SERIES
Integrated Circuit
Logic Modules

CONTENTS

Publication No. 64–51–13B


Ceramic package ensures positive hermetic seal.
Four pins reserved for ground substantially reduce ground line noise.
Dense packing reduces equipment size.
Popular DTL dual-in-lines are used for economy.
Ten test points are available at front edge.
Four 2-in NANDs in each IC package.
52 ribbon connectors (26 each side) for easy access to all circuits.
All components clearly identified.
Individual power line filter on each module.
1
2
3
4
5
6
7
8
9
10
LJ10 2 IN GATE ASSY 145144 SER
© SDS-67
Actual size 4 1/4 x 4 3/4.
Epoxy-glass mounting board.

J SERIES : A COMPLETE MODULE FAMILY

J Series is a complete family of low cost logic and analog modules, cabinets, power supplies, and cabling, for the system engineer. J Series provides a choice of industry standard DTL or TTL IC logic circuits, together with high performance supporting circuits such as logic-level shifters, clock oscillators, Schmitt Triggers, and many others. Most J Series modules with DTL circuits are also provided in a TTL version with identical logic functions and exact module pin compatibility.

To help each user build precisely the right system at lowest cost, J Series also provides a complete selection of do-it-yourself dual-in-line socket modules, breadboard, and blank modules.

To help each user check out and troubleshoot the system quickly, J Series has a new front-edge test lamp assembly that mates with test points provided on the logic modules.

And to help each user design in least time, SDS provides engineering advice with each order, the unique Automated Wire Listing service, and Automated Wiring service when needed.

HOW COMPLETE?

Right now, J Series includes seventy-eight module types, four kinds of power supplies, twenty-six cabinet and mounting case models, and seven cabling models. Of these one-hundred and fifteen products, fifty-four are offered for the first time in this catalog. J Series is open ended; it continues to grow as new products are needed.

HERE IS THE CURRENT LIST OF MODULES

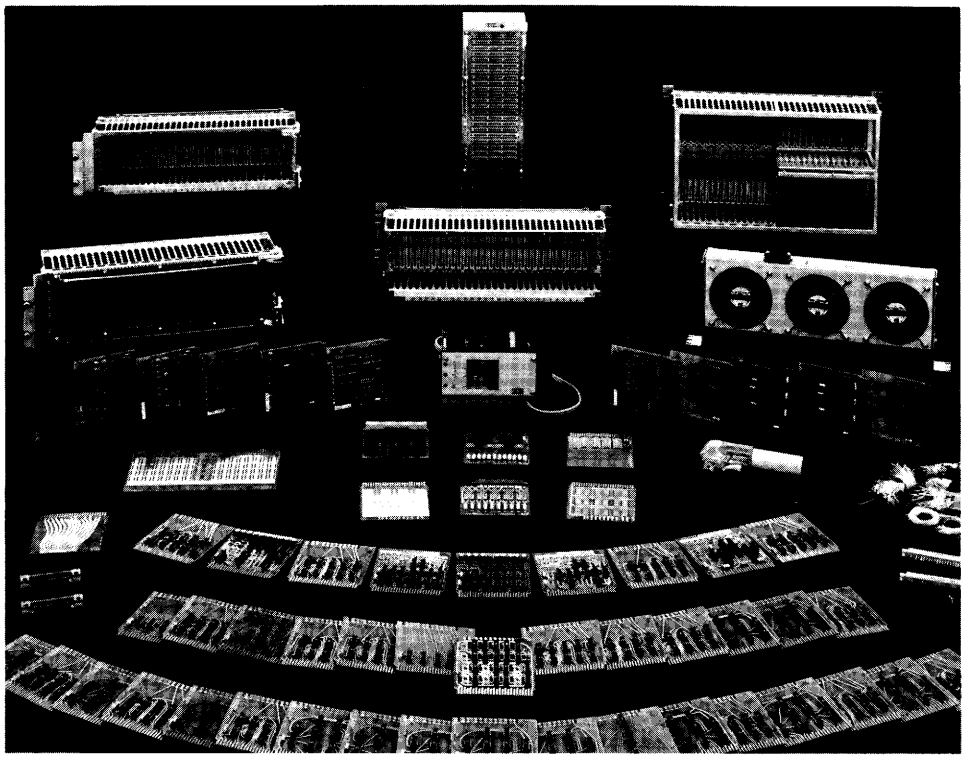
FUNCTIONAL MODULES		IC TYPE
BJ10*	10-line decoder and lamp driver	DTL
BJ11*	16-line decoder	DTL
BJ12*	10-line decoder, 3 decades BCD	DTL
BJ60*	10-line decoder and lamp driver	TTL
BJ61*	16-line decoder	TTL
BJ62*	10-line decoder, 3 decades BCD	TTL
FJ11	4-bit bidirectional counter-register	DTL
FJ13	4-bit storage registers (16 bits)	DTL
FJ14*	Dual 8-bit shift registers	DTL
FJ16*	BCD counter/decoder	DTL
FJ17*	Binary counter/decoder	DTL
FJ18*	BCD counter, 3 decades	DTL
FJ19*	Dual 8-bit storage registers	DTL
FJ20*	Dual 10-bit storage registers	DTL
FJ21*	Dual 12-bit storage registers	DTL
FJ61*	4-bit bidirectional counter-register	TTL
FJ63*	4-bit storage registers (16 bits)	TTL
FJ64*	Dual 8-bit shift registers	TTL
FJ66*	BCD counter/decoder	TTL
FJ67*	Binary counter/decoder	TTL
FJ68*	BCD counter, 3 decades	TTL
LJ11	Digital multiplexer	DTL
LJ16	4-bit parallel binary adder	DTL
LJ61*	Digital multiplexer	TTL
LJ66*	4-bit parallel binary adder	TTL

TIMING MODULES		CIRCUIT TYPE
CJ16	Clock, 7.8 KHz to 2 MHz	Discrete comp.
CT10	Clock, 1 MHz to 10 MHz	Discrete comp.
OJ14*	4 one-shots (50μsec to 2.2sec)	Discrete comp.
OJ18	4 one-shots (100nsec to 20μsec)	Discrete comp.

FLIP-FLOP MODULES		IC TYPE
FJ10	J-K flip-flops	DTL
FJ12	Universal flip-flops	DTL
FJ60*	J-K flip-flops	TTL
FJ62*	Universal flip-flops	TTL

ANALOG AND REGULATOR MODULES		CIRCUIT TYPE
DJ24*	D-to-A converter	Discrete comp.
HT58*	Universal operational amplifier	Discrete comp.
HT72*	General purpose amplifiers	709 linear amps
WT49*	±35v regulator	Discrete comp.
WT53*	±25v regulator	Discrete comp.
WT54*	±15v regulator	Discrete comp.

* Offered for the first time in this catalog.



The J Series Logic Module Family

GATE MODULES		IC TYPE
IJ10	2-in NANDs	DTL
IJ11	3-in and 4-in NANDs	DTL
IJ12	2-in NANDs; inverters	DTL
IJ13*	2-in power NANDs	DTL
IJ14*	2-in power NANDs	DTL
IJ16*	4-in power NANDs	DTL
IJ60*	2-in NANDs	TTL
IJ61*	3-in and 4-in NANDs	TTL
IJ62*	2-in NANDs; inverters	TTL
IJ64*	2-in power NANDs	TTL
IJ66*	4-in power NANDs	TTL
LJ12	Exclusive-ORs	DTL
LJ17*	8-in NANDs	DTL
LJ62*	Exclusive-ORs	TTL

DRIVER AND INDICATOR MODULES		CIRCUIT TYPE
QJ17*	Indicator module	Discrete comp.
RJ10	Lamp and relay drivers	Discrete comp.
XJ11*	Test lamp assembly	Discrete comp.

* Offered for the first time in this catalog

THRESHOLD DETECTING AND LEVEL SHIFTING MODULES		CIRCUIT TYPE
AJ10*	Cable receivers	DTL + discrete
AJ11*	Cable drivers/receivers	DTL + discrete
AJ12*	Cable drivers	DTL + discrete
AT22	Schmitt triggers	DTL + discrete
AT69*	Differential receivers	Discrete comp.
HT73*	Voltage comparators	Discrete comp.
NT18	Negative logic-to-SDS	Discrete comp.
NT33*	SDS-to-negative logic	Discrete comp.

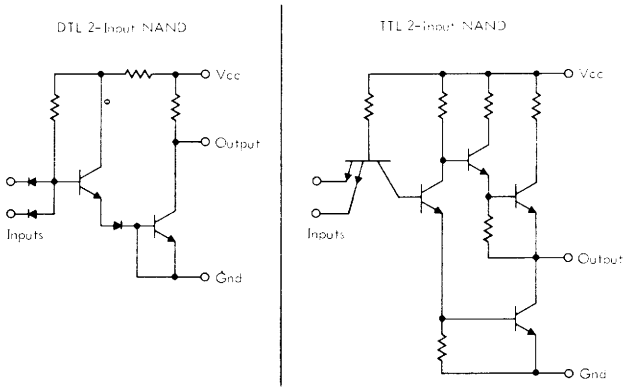
ACCESSORY MODULES	
ST14	Manual toggle switches
XJ10	External pull-up resistors
XJ12*	MSI blank module (for 3 dual-in-lines)
XJ13*	MSI blank module (3 TI dual-in-lines)
ZJ10*	Socket module
ZJ12*	Breadboard module (8, -14, -16-lead)
ZJ14*	2-high Socket module (14, 16-lead)
ZT11	Blank module
ZT15	Cable plug (solder connections)
ZT23	Cable plug (pressure contacts)
ZT37	Breadboard module (dual-in-lines or TO5)
ZT53	Extender module
ZT60*	Copper-clad blank module

CHOOSE YOUR CIRCUIT - DTL OR TTL

Most J Series logic modules are available in two versions: DTL (Diode-Transistor Logic) and TTL (Transistor-Transistor Logic). These are pin-for-pin compatible; that is, the logic functions performed on each module are the same, and the same inputs and outputs are available at the same pins. You can now choose either DTL or TTL characteristics, and be sure that the logic design is identical down to the pin number.

WHAT'S THE DIFFERENCE?

DTL and TTL circuits have different operating characteristics due to structural differences. The TTL circuit used in J Series contains three more transistors than the equivalent DTL circuit. One transistor substitutes for the input diode gate structure, replacing the diodes with multiple emitters. The other two transistors work as a pair, substituting an active pull-up circuit for the simple 6K ohm pull-up resistor found in the DTL circuit. The effective pull-up resistance of the TTL output, when the upper output transistor is in the ON condition, is less than 100 ohms.



The differing circuit structures lead to performance differences in four main areas: speed (clock rate), noise level, power consumption, and logic flexibility. J Series modules exhibit differences in only three of these areas: speed, power, and logic flexibility, because special precautions have been taken to reduce noise.

SPEED

DTL performs best in systems with clock rates up to 5 MHz, while TTL operates reliably up to 20 MHz. The faster TTL speed results from three factors:

1. The lower output pull-up impedance greatly reduces rise time because parasitic capacitance on the signal line can charge more quickly.
2. The multiple-emitter input configuration has less input capacitance than the diode configuration. Less capacitance is therefore placed on each signal line, further improving rise time.
3. Internal propagation delay is less than with DTL.

POWER CONSUMPTION

TTL circuits consume about 10% more power than DTL. However, except in large systems, the difference can usually be neglected because the power used by both types is small.

LOGIC FLEXIBILITY

DTL outputs can be connected together to form "wired" logic structures. When one DTL output goes to zero volts, it holds the signal line at ground potential regardless of the state of other outputs on the line. The only electrical effect is to draw additional current through the 6K ohm pull-up resistors on the line. Thus DTL is short-circuit proof.

TTL, on the other hand, is not short circuit proof; the pull-up transistor can burn out. Therefore, TTL wired logic is not allowed.

A second advantage of the slower DTL is relative immunity to clock skew. When delays are short, as with TTL, the allowable difference between arrival times of clock signals becomes correspondingly short. Otherwise, erroneous triggering due to logic races can result. Consequently, more care is required in designing the clock system and the interconnecting wiring when TTL circuits are used.

More information on these logic design considerations is available from SDS in the form of application bulletins.

MODEL NUMBERS

Note that compatible modules always carry related model numbers. To obtain the TTL number, add 50 to the DTL number.

CONCLUSIONS

Use DTL for economical low speed and medium speed, minimum power consumption applications. Use TTL for high speed applications, where slightly higher cost and the lack of "wired-output" logic are not critical factors. SDS mechanical and electrical compatibility allows you to use both types in combination, to gain the advantages of both.

NOISE PROTECTION

SDS features extra noise protection on all TTL modules to guarantee that noise levels on signal lines will be well below worst-case switching thresholds, and to prevent transients from coupling through the power/ground circuit. These objectives are achieved with a shield plane laminated into every TTL printed circuit board, plus liberal use of decoupling capacitors at power distribution points.

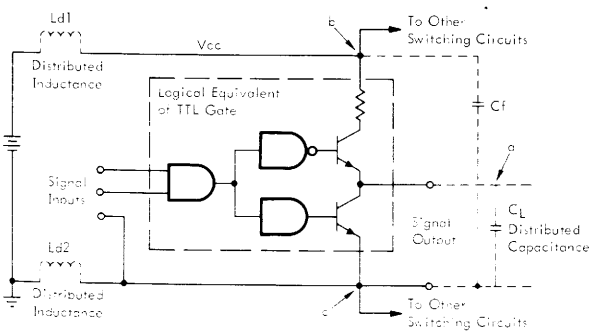
A RESULT OF FAST SWITCHING

Faster switching, attainable with TTL circuits, increases the amplitude of voltage spikes that can appear at power and ground connection points.

Consider the combination of a power source, TTL circuit, and ground return path, shown in the diagram. Each time that the action of the switching circuit causes a surge of current to be drawn from the power source, a voltage spike can appear between Vcc and ground connections, because a current surge causes a voltage drop across the distributed inductance of the power supply/ground circuits. These spikes may be coupled to all other circuits through the power and ground busses. When they are sufficiently large to exceed the TTL noise immunity, erroneous triggering can occur.

A surge of current can be drawn from the power source in two ways. When the output logic level rises, current is needed to charge load capacitance C_L. Secondly, with TTL, simultaneous conduction of both output transistors is possible during switching. This can provide a path for current flow directly from Vcc to ground, while both transistors change state.

The resulting voltage transient is proportional to inductance and to the rate of change of current: $V = L\ (di/dt)$. As can be seen from this equation, V can be reduced only by reducing L, or by reducing di/dt, or both. SDS eliminates this potential problem by reducing both.



REDUCING THE EFFECTIVE di/dt WITH DECOUPLING CAPACITORS

Consider in detail the action of the switching circuit upon the power and ground lines, at terminals b-c. When the output is switched to high, the capacitance C_L is charged by a surge of current from the power system.

If current can be supplied instead from some point within the switching circuit, then the di/dt seen at terminals b-c is less, and the voltage transient is smaller.

If a capacitor, Cf, is placed between terminals b-c, it will store a charge proportional to Vcc. When the switched output goes high, some of the current required to charge C_L is drawn from Cf instead of the power bus. This reduces the rate of change of current (di/dt) in the power/ground circuit, and proportionately reduces the size of the voltage transient at terminals b-c. Cf has the same beneficial effect when both output transistors conduct simultaneously.

All SDS J Series TTL modules have a .01μfd capacitor between the Vcc connection point and ground, for every three TTL circuits. An additional 1.5μf capacitor is placed where the Vcc bus enters the module. These hold sufficient energy to easily suppress the transients generated on the module, and keep them out of the power system.

REDUCING L WITH A GROUND PLANE

Now consider the effect of layout on distributed inductance.

The wider the physical spacing between a power supply conductor and its ground return conductor, the higher will be the inductance of the loop formed by the two conductors. Shielded or twisted-pair wire can reduce the spacing, (and inductance), but is impractical for use on circuit boards.

Instead, SDS uses a ground plane which is a thin sheet of copper, coplanar with the circuit etch. The ground plane decreases inductance because an image current is induced in the ground plane which confines the magnetic field associated with circuit current to a relatively small volume. In effect, circuit current flows in a strip transmission line instead of a high-inductance loop.

CONCLUSION

The use of additional decoupling capacitors and a ground plane effectively suppresses power supply transients which normally result from the faster switching of TTL. Therefore, J Series TTL modules and DTL modules operate in substantially the same noise-free environment.

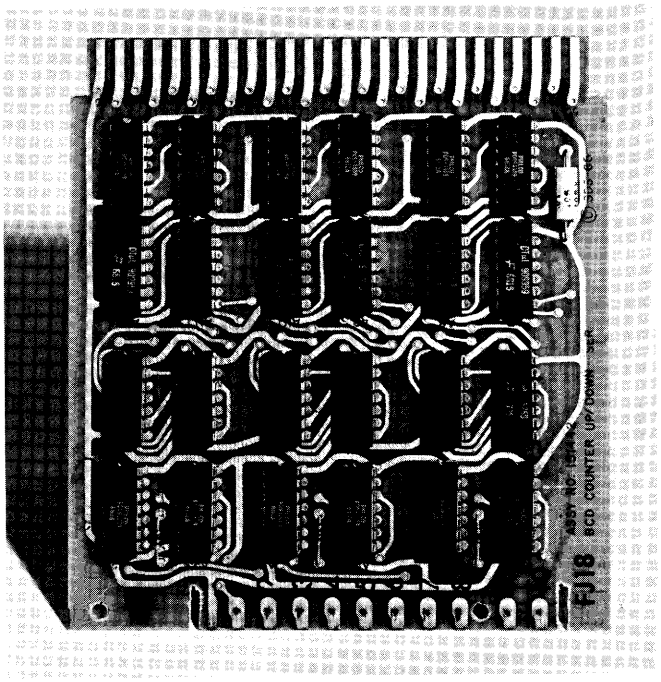
FUNCTIONAL MODULES

As can be seen from the listing of J Series modules on page 2, SDS offers more functional modules than any other single type. These modules contain a complete assembly of gates and flip-flops (as required), interconnected with circuit etch into basic logic blocks: counters, registers, decoders, adders, etc.

Functional modules conserve the system budget in four important ways:

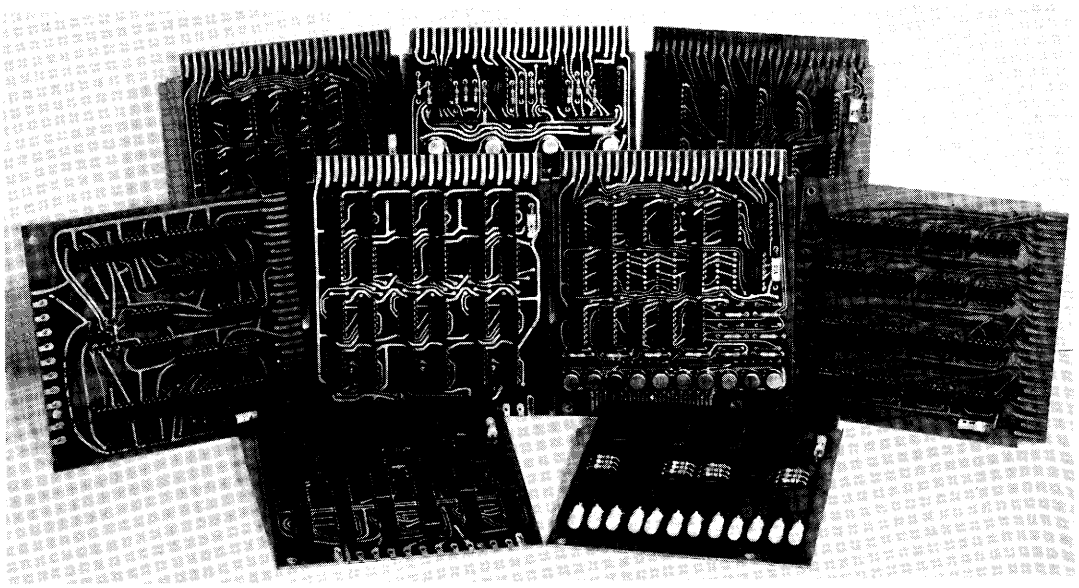
1. They save design time. The most popular logic block configurations have been implemented once and for all.
2. They save space in the mounting case.
3. They save the cost of interconnecting backplane wiring.
4. They save time during system checkout, and are easier to troubleshoot.

Take the FJ18 for example. Here three decades of BCD counting are packed on one module. With this kind of density, card count is greatly reduced, saving design time, wiring time (and wiring errors), and checkout time, as well as floor space and mounting hardware.



FJ18 BCD Counter - three decades of bidirectional BCD counting.

Typical Functional Modules



SPECIAL CIRCUITS

Special circuits such as interface circuits, cable drivers, Schmitt Triggers and various types of analog modules are often hard to get. But SDS offers a wide variety of these modules, from stock. Many are adapted from the large inventory of proven SDS system module designs which have been developed during the past three years of intensive IC computer system engineering. Some were expressly designed for the J Series module line, to assure that all of the most needed special functions are available.

Among the most popular modules are:

AJ10, AJ11, AJ12 -- Three cable driver and receiver modules with provision for directly attaching cables to the module. Cables up to 3,000 feet long can be reliably driven at high speed with these specially designed circuits. A combination of integrated and discrete components provides capabilities that cannot be matched in any other way.

OJ14, OJ18 -- A pair of one-shot modules which provide a range of accurate, adjustable single timing pulses from 100 nanoseconds to 2.2 seconds. Each module contains four independent circuits.

AT22 -- A Schmitt Trigger module with two independent circuits. Each circuit has two adjustable thresholds. When the input crosses one threshold the output goes True; when it reverses and crosses the other, the output goes False.

CT10, CJ16 -- Two stable, crystal or adjustable LC controlled clock oscillators, which completely cover the range 7.8 KHz to 10 MHz.

NT17, NT18, NT33 - Three interface modules which allow the J Series circuits to interface with negative logic. The NT33/AT69 pair provides a direct interface with Univac and CDC equipment.

HT58 -- A new high performance Universal Operational Amplifier module whose circuit configuration and feedback path can be changed to create many varieties of Op Amps or buffers.

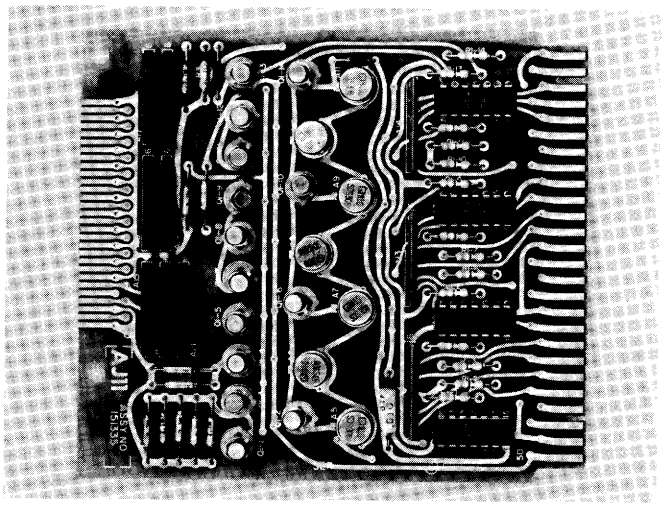
DJ24 -- This module converts 9 bits and sign to ±10v, ±20 ma analog output with an accuracy of 0.1%. Digital storage, if needed, may be provided with a separate module (FJ20).

WT49, WT53, WT54 -- Three regulator modules with ±35v, ±25v, and ±15v outputs, at 1% or better accuracy.

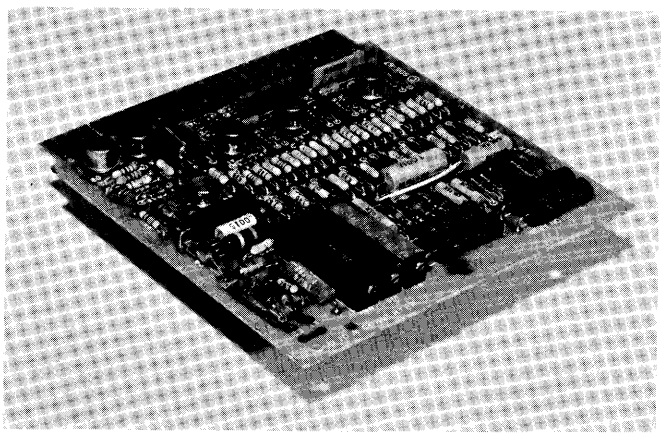
HT72 -- One module containing two economical general purpose Op Amps based on the familiar 709 integrated linear amplifier, with beefed-up output and gain regulation.

HT73 -- A voltage comparator module with nine independent circuits. Each provides a logical output to indicate when one voltage input exceeds the other.

These modules, and others described in Section II, are time savers because they provide ready-made solutions to most special-function problems. The J Series user has the added advantage of knowing that many other proven designs are available from other SDS module lines which can be adapted to almost any situation not covered here. And, the J Series engineering staff is always available to create new designs to order.



AJ11 Cable Driver-Receiver



DJ24 Digital-to-analog Converter

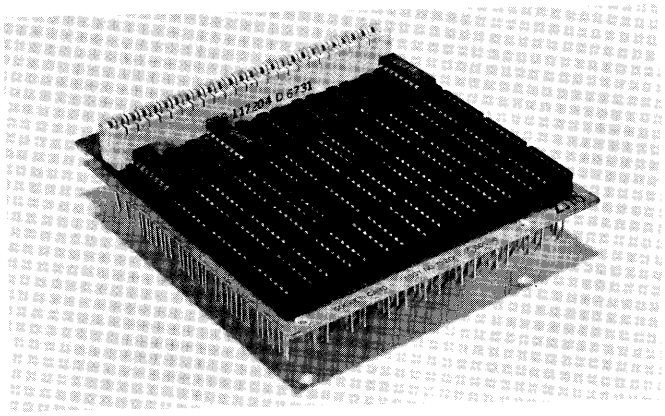
CUSTOM MODULES MADE EASY

Custom modules are unique modules made by the user or made by SDS for the user. The system engineer may need a custom module in one or more of these situations:

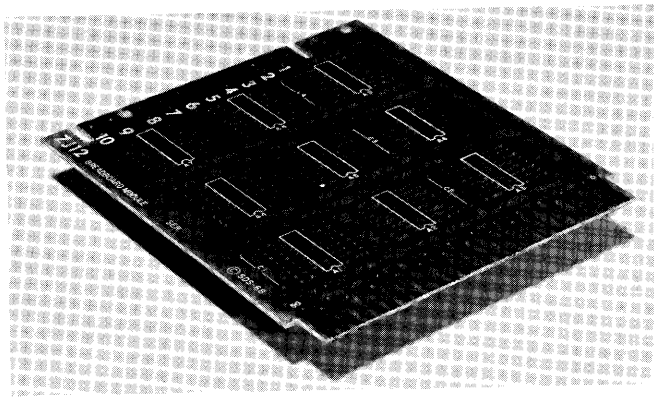
1. He needs to place several complex-function (MSI) dual-in-line circuits of different types on the same module to achieve close interconnection.
2. A small portion of the logic system is in the development phase and frequent changes in both wiring and logic may be needed.
3. The logic system is so small that it can fit entirely on one or two circuit cards.
4. He needs to build a unique circuit using a mixture of IC and discrete components.
5. He needs to build a special module to implement the few logic functions that are left over when a logic design is almost complete.
6. He contemplates volume production of a logic system. In this situation, it is often desirable to design custom logic arrays, which are then manufactured in quantity, either by the user or by SDS.

SDS offers a variety of accessory modules to meet these needs.

- The XJ12 MSI Blank module contains drilled mounting spaces for three 16-lead dual-in-line packages. Each dual-in-line lead is connected to one back-panel ribbon connector via etch, making all leads of the three packages available at the back panel. A ground plane for noise protection is placed on one side of the board.
- The ZJ10 Socket module makes it possible to plug in 32 dual-in-line packages and obtain reliable connections without solder. IC's can be changed at will. Interconnecting wiring is also changeable: wire-wrap posts are provided on the back of the module, and connections may be wrapped or may be made with VT10 push-on connectors. A standard VT11 wire-wrap connector is installed near the back edge, to provide wrap posts for convenient connection of wire to the ribbon connectors at the back of the card.
- The ZJ12 Dual-in-line Breadboard module contains nine drilled mounting locations for 8-, 14-, and 16-lead packages. The IC's are inserted and soldered in place. Interconnections are made with jumpers soldered to plated-through holes in the etch.
- The ZT11 Blank module is useful when building special circuits with discrete components which vary in size, where interconnections will be made with jumper wires. The module consists of an undrilled epoxy-glass board with gold-plated copper foil ribbon connectors along the back edge, but no other copper foil.
- The ZT37 Breadboard module is similar to the ZJ12, but is drilled and etched for mounting and soldering discrete and TO-5 package components as well as 14-pin dual-in-lines.
- The ZT60 Copper Clad blank is similar to the ZT11, but has solid sheets of gold-plated copper foil attached to both sides. The board can be drilled and etched as desired. It is useful for making limited production runs of special modules.
- SDS also offers unstuffed modules at nominal cost.



ZJ10 Socket Module



ZJ12 Dual-in-line Breadboard Module

CUSTOM SYSTEMS MADE EASY

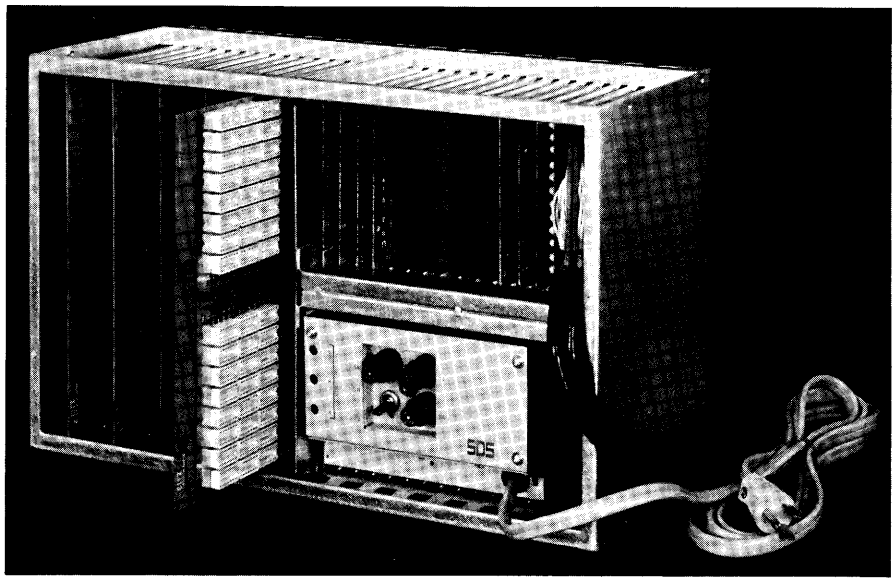
Shown on this page are two SDS product innovations. One is a new board, and the other a new mounting case.

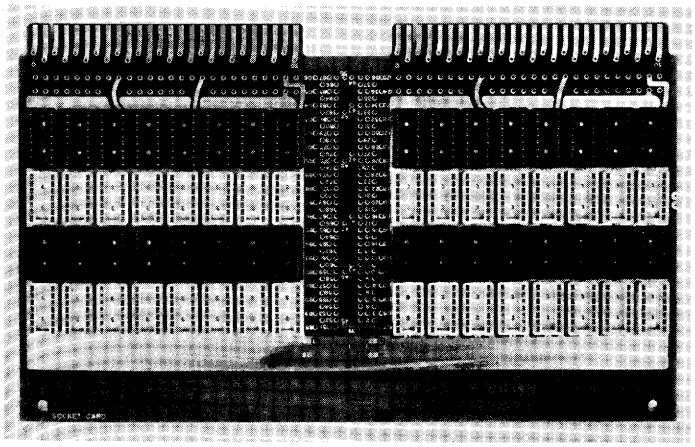
The new board is a double-height socket board, which can hold up to 64 dual-in-line MSI, gate, or flip-flop packages, and provides wrap pins for all connections.

The mounting case has a double-height section for five of the socket boards, and two sections for standard SDS modules (or compact PT10 power supplies). Backplanes with wire-wrap pins, ground planes, and power connections are provided as usual. Request the Model MT42 mounting case.

Now you can build a whole custom system, containing power supplies, standard modules, MSI circuits and all, within one compact 10-1/2 inch by 8 inch by 19 inch container. Or, let SDS wire and assemble the system for you, to your logic design.

If the custom system is to become a production model, SDS can create double-height etched boards in production quantities at reasonable cost. The mounting case will hold up to sixteen double-height etched boards with directly mounted dual-in-line ICs as well as fifteen single-height boards.





Advantages of the new ZJ14 socket board:

- High density packing.
- Simple, low cost IC replacement.
- Inventory economy--plug in ICs only when needed.
- Low noise--ground planes in boards and mounting case greatly reduce effects of switching transients.

UNIQUE SIGNAL TRANSMISSION TECHNIQUES

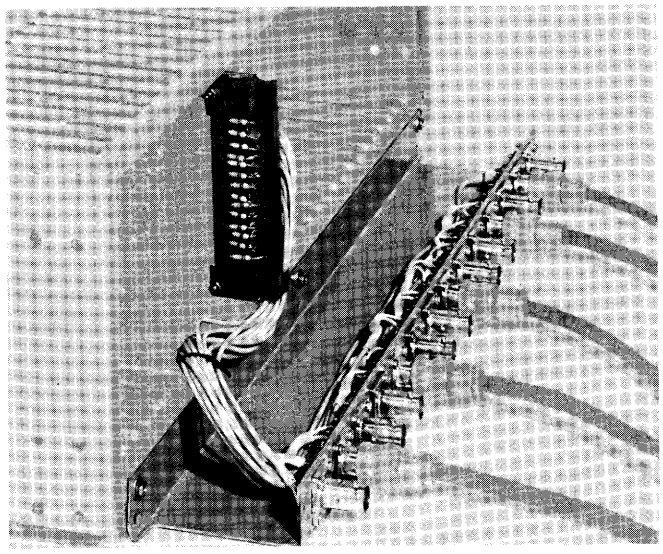
Take a signal from A to B. How much it is distorted depends on the nature of the path and the distance traveled. Some transmission paths protect the signal more than others; an ideal path shields the signal from all external influences, and delivers it intact.

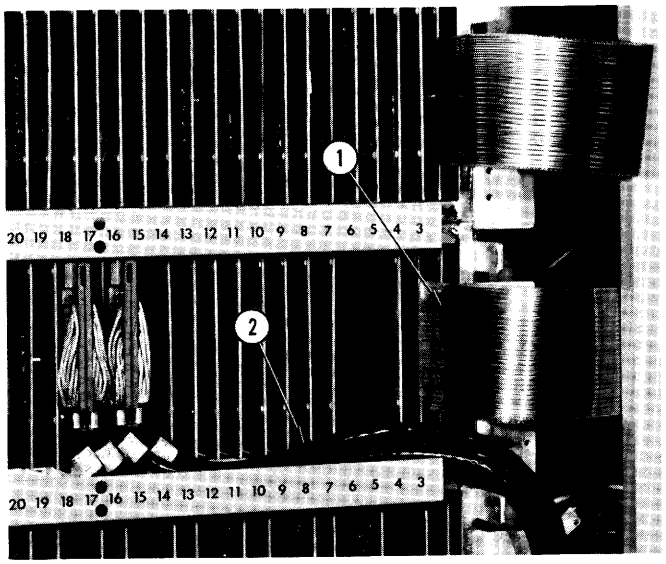
SDS wiring and cabling hardware was developed for large systems, where the possibilities of distortion are magnified. These drivers, receivers, and cables can take a signal over longer distances, with less distortion. They deliver the signal intact.

SDS ribbon cabling (1, in photo at right) allows you to drive logic signals up to 115 inches, directly from logic outputs to logic inputs, and maintain signal integrity. The ZT45 and ZT46 units described in Section 3, carry up to 48 signals paralleled by ground-return lines, through a 104-line, 100-ohm flat ribbon cable.

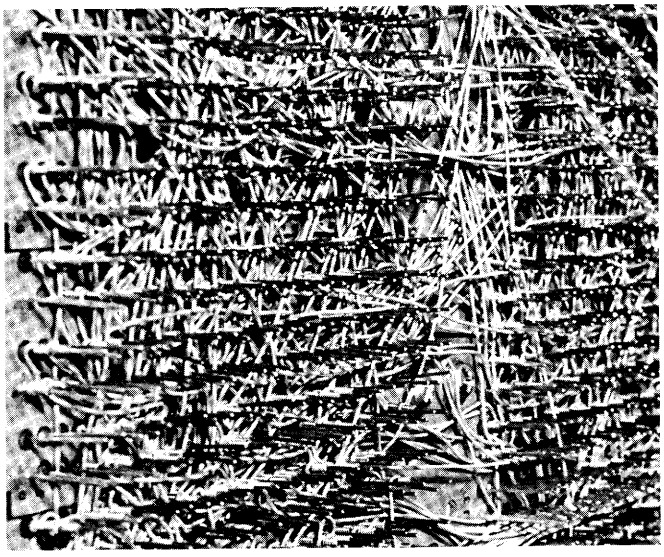
Coaxial shielded 14-conductor, single bundle Model ET12 33-ohm cabling (2 in photo at right) is suitable for distances up to 200 feet. AJ10, AJ11, AJ12 Cable Driver and Receiver modules are used, and the fourteen cable ends in each bundle are fastened to the module with a simple quick-disconnect mechanical device.

For even longer distances, up to 3,000 feet, use 93-ohm coaxial cable and the ET24 BNC Connector Assembly. Drive and receive the signals with the same AJ10, AJ11, AJ12 modules used for 33-ohm cable.





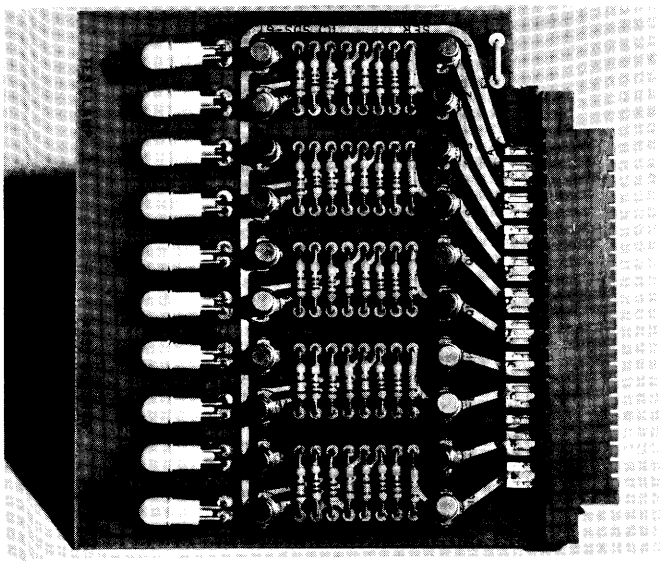
The ZT52 wire used to interconnect backpanel wire wrap pins has two special mechanical features. The insulation is especially tough, to resist cold flow; and, the copper conductor has the proper tensile strength to provide a firm wrap without loosening the pin. Electrically, the wire behaves as a 150-ohm transmission line, when pushed close to the ground plane that is built into all SDS mounting cases. The ground plane protects the signal.

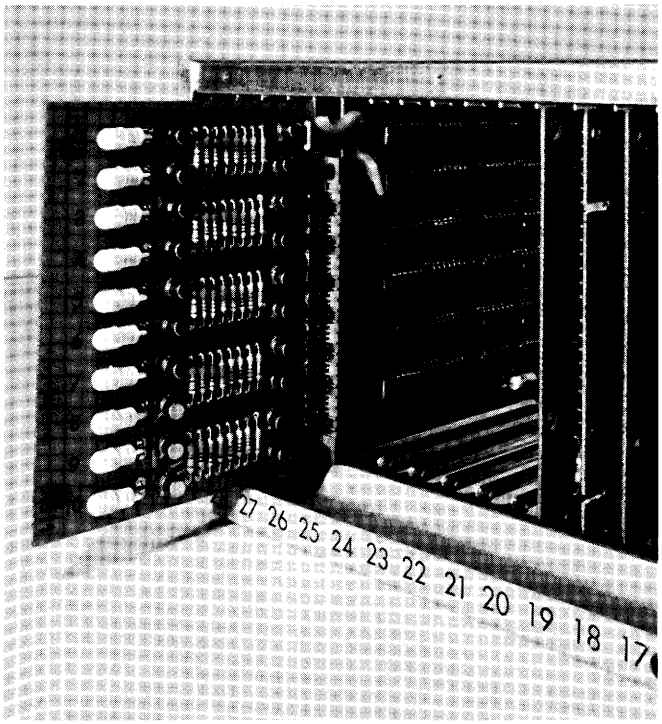


NEW TEST LAMP ASSEMBLY

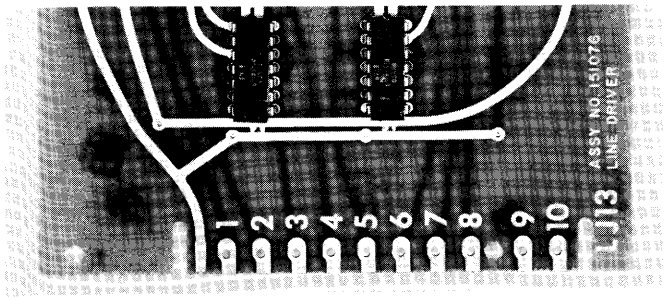
How do you monitor, all at once, the important logic level changes in a module under test? Simply place the XJ11 Test Lamp Assembly over the convenient test points provided on each J Series logic module. Now the logic levels are clearly displayed, simultaneously, visible even under ordinary room lighting. When the module is slowly stepped through its operating sequence an incorrect pattern is apparent right away. The XJ11 eliminates the chore of moving scope leads from point to point and recording the results on paper.

Ten bright test lamps are mounted along the assembly's front edge. A special socket is mounted at the back edge. When this socket is placed over a logic module front edge it connects the lamp drivers to test points and to power and ground.





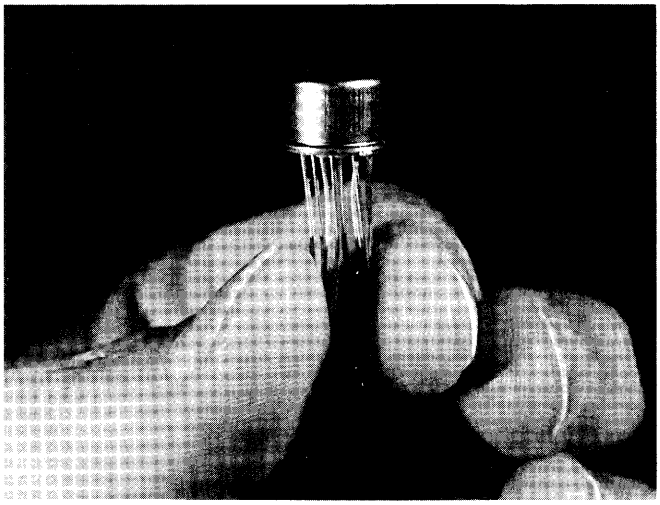
Each logic module has up to ten test points on its front edge. These are internally connected to critical nodes such as logic circuit outputs. Each test point has a plated-through hole to hook a scope probe. A pair of slots assures proper alignment of the XJ11 Test Lamp Assembly with test points.



IC RELIABILITY

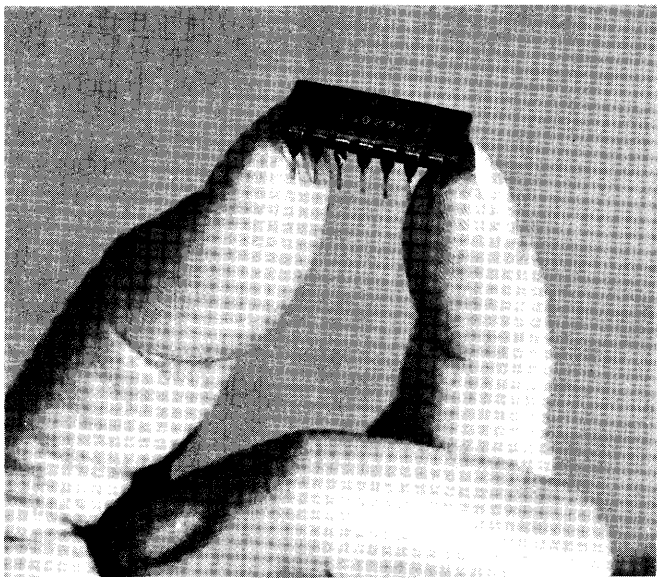
Low initial cost is never sufficient excuse to risk the reliability of a data processing system. The potential expense of inaccurate results, lost time, and needless maintenance are always greater than the small additional investment needed to assure state-of-the-art reliability.

For this reason SDS uses only ceramic dual-in-line and metal TO-5 can packages, in preference to the less expensive plastic. Both the ceramic and TO-5 package types have a well known, consistent record of high reliability. Conversely, some questions continue to be raised about the long-term stability of metal-to-plastic seals, the possibility of moisture deposit formation inside the plastic package during manufacture, and the adequacy of plastic for use in high temperature or high humidity environments.



At a recent conference among semiconductor manufacturers, industry users, and government representatives from NASA, DOD, and the three military services, the consensus among government officials was that plastic encapsulated devices could not be recommended for space or military use.

Accordingly, SDS J Series modules are made with ceramic and TO-5 packaged ICs, the only packaging techniques that meet SDS standards.

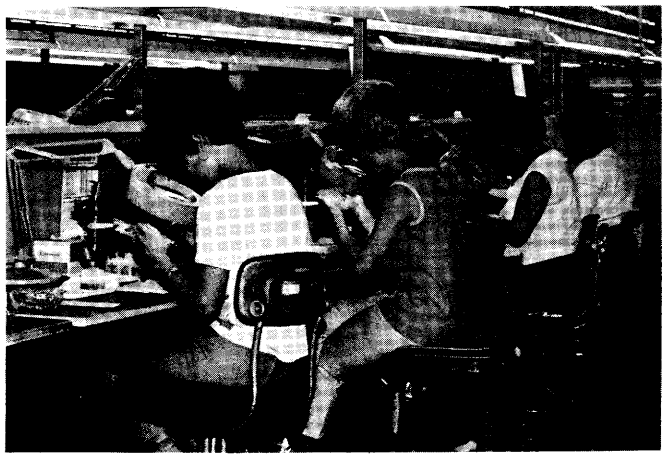


MAKE OR BUY?

The cost/performance tradeoffs involved in the decision to make or buy modules are often poorly understood. Usually the costs of producing modules in low volume are greatly underestimated. Performance problems also arise due to lack of experience with the subtleties of circuit board layout and manufacture. Many engineers, after having been caught behind schedule and overbudget, have decided that their time is better spent on system design and checkout. They have found that it pays to take advantage of the module maker's expertise.

SDS offers these benefits with its J Series module family:

- A wide choice of well planned module types with compatible DTL and TTL circuits is provided.
- Your engineering time is reduced: logic design, mechanical design, interconnecting wiring methods design, and manufacturing techniques have been thoroughly worked out. There is no need to duplicate work already done.
- Performance parameters have been matched: logic mix, loading, frequency response and delay times, noise rejection, power requirements, reliability and ambient specifications have all been considered in detail and the designs optimized.
- Special modules can be designed and built to your specifications by the SDS module engineering staff.
- Supporting circuits such as Schmitt Triggers and D-to-A modules have been developed over periods long enough to assure consistent reliability. These tricky circuits often become the most troublesome and time-consuming items of an in-house design project.
- Quick delivery is standard. Orders are usually filled shortly after receipt of order. Compare this with the months of lead time required to produce a new product.
- Experienced quality control is exercised during manufacture. One year warranty is standard. A complete module repair facility is also available to SDS module users.
- A full choice of accessories, mounting hardware, power supplies, and cabling is offered. Many of these items would be considered too costly in a "make" situation.
- Application engineering and thorough documentation are provided. The documentation alone would be too costly to create for a one-time effort.
- Automated Wire Listing service and Automated Wire Wrapping service are now available to SDS module users.



A Portion of The SDS Module Production Line

This integrated circuit tester is controlled by an SDS 92 computer that accepts or rejects circuits being tested and keeps a record from which engineers can evaluate the quality of circuits supplied by various vendors. Only a large volume module manufacturer can support testing on this scale.

SUMMARY OF SPECIFICATIONS

	SPECIFICATION	UNITS	DTL			
			NAND	FLIP-FLOP	944 POWER NAND	932 POWER NAND
SUPPLY VOLTAGE AND POWER	Supply voltages	volts, dc	+5 volts, ±10% (Absolute maximum +8v for Vcc)			
	Power consumption, typ.	mw	9	47	23	29.5
	Power consumption, max.	mw	14	57	29	36.5

LOGIC LEVELS AND NOISE IMMUNITY	High logic level, acceptable input range	volts, dc	+2.6 to +5.5
	High logic level, max. output range	volts, dc	+2.6 to +5.5
	Low logic level, acceptable input range	volts, dc	0 to +0.4
	Low logic level, max. output range	volts, dc	0 to +0.4
	Switching threshold, nominal	volts, dc	+1.5
	Noise immunity, typical, at low freq., 25°C	volts, peak	1
	Noise immunity, worst case, at low freq., 25°C	volts, peak	0.7

LOADING AND FAN-OUT	Sinking current at output, absolute max.	ma	30	30	100	100
	Unit load, typical	ma	1.1			
	Unit load, max.	ma	1.6			
	Input loading	unit loads	1	S:2/3 R:2/3 C:2 SD:2 RD:2	1	1
	Fan-out (Output driving capability), same logic family	unit loads	8	10	25	25
	Fan-out (Output driving capability), opposite logic family	unit loads	1 (w/o pull-up) 4 (with 1.1KΩ)	1 (w/o pull-up) 4 (with 1.1KΩ)	9 (with 1.1KΩ) 19 (with two parallel 1.1KΩ resistors)	25

TTL				NOTES	
NAND	FLIP-FLOP	POWER NAND	AND/NOR		
+5 volts, ±10% (Absolute maximum +8v for Vcc)				+8v ±10%, and -8v ±10% are also required for some special function modules	SUPPLY VOLTAGE AND POWER
9	75	30	13	TTL power is frequency-dependent. Max. power is given at max. frequency and max. supply. Power is averaged over both the high and low states. DTL power is not frequency-dependent.	
61	151	165	84		

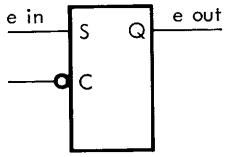
+2.4 to +5.5		LOGIC LEVELS AND NOISE IMMUNITY
+2.4 to +5.5	Low value is output at full load, worst case IC, low supply. High value is output at no load, high supply.	
0 to +0.4	Typical low logic level is +0.2 volts. Do not go more negative than 0.0v.	
0 to +0.4		
+1.5		
0.9	TTL transient noise immunity (high freq. noise immunity) is better than DTL because of low output impedance in both states, which reduces capacitive coupling.	
0.5		

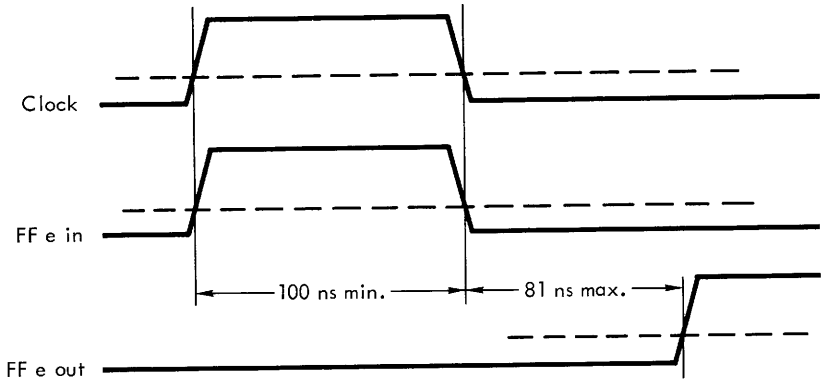
50	50	100	50		LOADING AND FAN-OUT
1.1				Unit load is measured at the low logic level, where maximum conduction occurs. Max. unit load value is used to calculate fan-out, for safety.	
1.6					
1	J:1 K:1 C:1 SD:2.7 RD:2.7	2	1	Each input loads the logic line with the number of unit loads shown. When DTL outputs are connected to form "wired logic", each additional output connected to the node contributes 5/6 unit load. TTL outputs cannot be connected to form "wired logic". Connect unused TTL inputs to +5v; otherwise, connect to active inputs, adding 1 unit load for each connection.	
10	10	30	10	DTL driving DTL or TTL driving TTL.	
10	10	30	10	DTL driving TTL, or TTL driving DTL. The low DTL to TTL fan-out is due to combination of TTL input leakage current with high DTL output impedance. This reduces logic high level below limit when more than 1 TTL input is driven. Reducing DTL output impedance with an external 1.1K ohm pull-up increases permissible loading.	

SPECIFICATION		UNITS	DTL				TTL			
			NAND	FLIP-FLOP	POWER NAND 944	POWER NAND 932	NAND	FLIP-FLOP	POWER NAND	AND/NOR
PROPAGATION DELAY	Propagation delay, typical	ns	31	51	36	41	10	17	15	15
	Propagation delay, worst case	ns	51	81	56	61	14	32	19	19
	NOTES	Delay is measured from threshold (+1.5v) to threshold, at 25°C, with standard test loads: DTL test load = 390 ohms || 30 pf; TTL test load = 15 pf.								

CLOCK SPECIFICATIONS

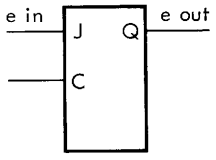
DTL

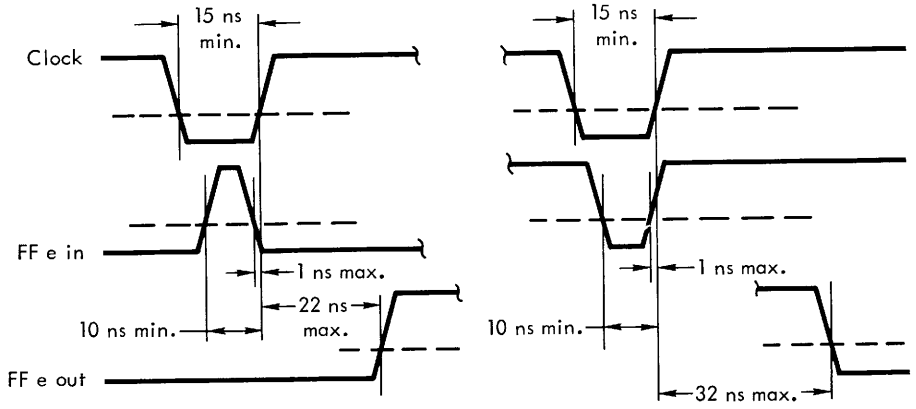




NOTES The clock must be high for 100 nsec min., during which time the inputs must be stable. The new output will be available 51-81 nsec after clock falling edge.

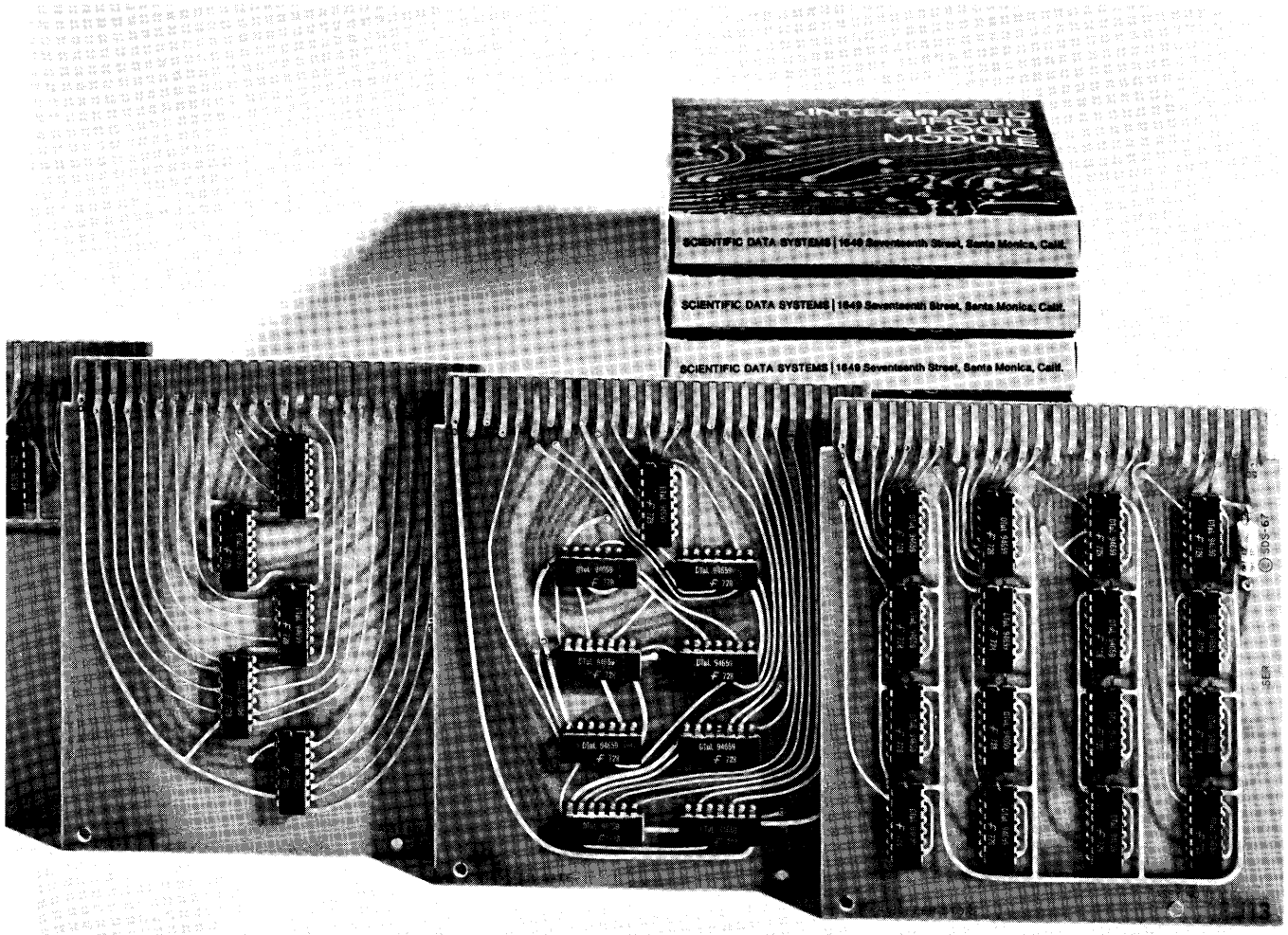
TTL





NOTES When the clock is low, the flip-flop inputs are enabled. When the clock rises, after being low for 15 ns min., the signal at flip-flop input is transferred into the flip-flop. The outputs then change state after a period corresponding to the propagation delay. Just before the clock rising edge occurs, the input signal must be stable for 10 ns min. (t set-up) and must remain in the desired state until at least 1 ns (t release) before the clock rising edge occurs.

MODULES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LOGIC SYMBOLS

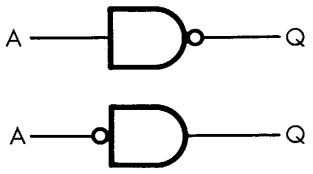
J Series logic and storage elements are represented by symbols based on MIL-STD-806B, as shown below. SDS uses the positive-True logic convention, where a signal is considered True (1) when high (nominal +5v) and False (0) when low (nominal 0v).

DTL CIRCUITS

NAND (Inverted AND)

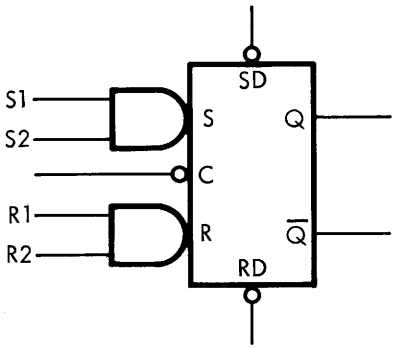
$Q = \overline{AB}$

INVERTER



$Q = \overline{A}$

CLOCKED, GATED RS FLIP-FLOP

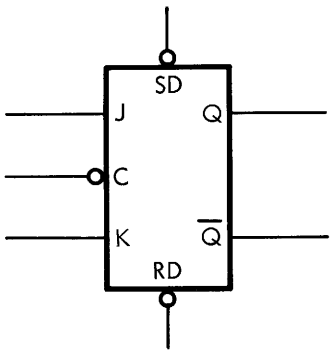


$S = S1 \cdot S2 \qquad R = R1 \cdot R2$

Before Clock					After *	
S	R	C (Clock)	SD	RD	Q	$\overline{Q}$
0	0	0	1	1	NC	NC
1	0	1 → 0	1	1	1	0
0	1	1 → 0	1	1	0	1
1	1	1 → 0	1	1	?	?
Any	Any	Any	0	1	1	0
Any	Any	Any	1	0	0	1
Any	Any	Any	0	0	1	1

* After clock, when all outputs have settled.
NC = No change.
? = Indeterminate

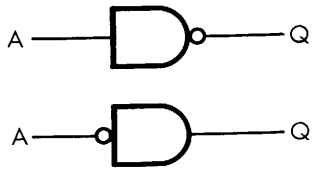
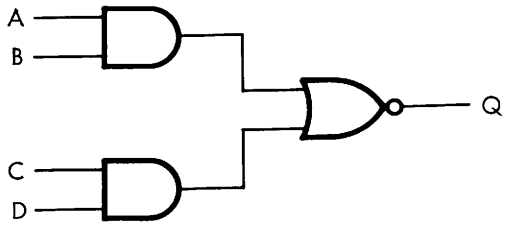
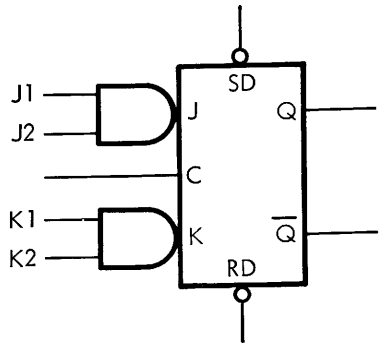
CLOCKED JK FLIP-FLOP



Before Clock					After *	
J	K	C (Clock)	SD	RD	Q	$\overline{Q}$
0	0	0	1	1	NC	NC
1	0	1 → 0	1	1	1	0
0	1	1 → 0	1	1	0	1
1	1	1 → 0	1	1	OP	OP
Any	Any	Any	0	1	1	0
Any	Any	Any	1	0	0	1
Any	Any	Any	0	0	1	1

* After clock, when all outputs have settled.
NC = No change.
OP = Opposite state from state before clock.

TTL CIRCUITS

FUNCTION	SYMBOL	LOGIC EQUATION OR TRUTH TABLE
NAND (Inverted AND)		$Q = \overline{AB}$
INVERTER		$Q = \overline{A}$
AND/NOR		$Q = \overline{AB + CD}$
CLOCKED JK FLIP-FLOP		$J = J1 \cdot J2$ $K = K1 \cdot K2$

Before Clock					After *	
J	K	C (Clock)	SD	RD	Q	$\overline{Q}$
0	0	1	1	1	NC	NC
1	0	0 → 1	1	1	1	0
0	1	0 → 1	1	1	0	1
1	1	0 → 1	1	1	OP	OP
Any	Any	Any	0	1	1	0
Any	Any	Any	1	0	0	1
Any	Any	Any	0	0	1	1

* After clock, when all outputs have settled.
NC = No change.
OP = Opposite state from state before clock.

AJ10, AJ11, AJ12
CABLE DRIVERS AND RECEIVERS

AJ10, AJ11, and AJ12 modules provide for high speed transmission and reception of logic level changes via a 33 ohm cable system, over distances up to 200 feet. The same modules can be used with a 93 ohm cable system and the ET24 BNC Connector Tray for distances up to 3,000 feet.

A cable with 14 individually shielded conductors can be clamped to either side of the front edge of one of these modules to mate with etched foil ribbon terminals. A second 14-conductor cable can be clamped to the other side of the front edge. Corresponding terminals on opposite sides of the front edge are connected together through the card. Thus two shielded 14-conductor cables (or 1 cable and a dummy load) can be connected to each module.

The Model ET11 cable connector must be used, and Model ET12 33-ohm cable is recommended for distances up to 200 feet. These components are described in catalog 64-51-15. For longer distances use 93-ohm cable and the model ET24 BNC connector tray.

One module type, the AJ10, contains 14 identical cable receivers; one (AJ12) contains 14 drivers; while the third (AJ11) has 14 pairs of driver-receiver circuits, each of which share a common pair of front-edge connectors. The AJ11 module reduces rack space and cable requirements in 2-way non-simultaneous communication by combining drivers and receivers on one card.

The AJ10, AJ11, and AJ12 modules are electrically compatible with the similar AT10, AT11, and AT12 modules, and provide a convenient method of interfacing J Series with T Series. However, there is a logical inversion in going through an AJ driver-receiver chain, but no inversion in going through the AT chain.

Cable Driver Circuit

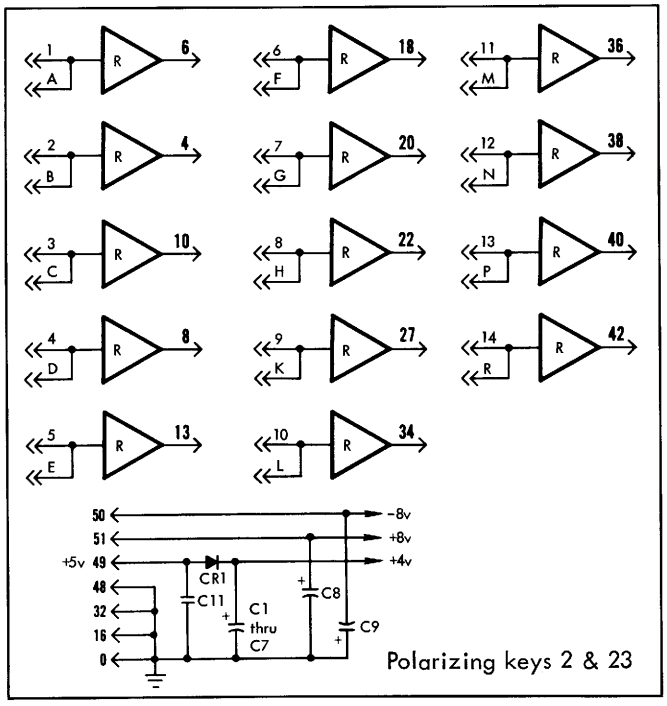
The cable driver circuit is preceded by a DTL inverter. It accepts standard J Series logic level input and converts level changes to nominal 0v and +2v logic level output, with inversion.

Driving capability depends on cable attenuation, which is a function of cable length and characteristic impedance. Any number of cable drivers can be connected to the same cable, but only one driver is allowed to be raised to the True (high) level at any given time, since output voltages are additive.

Cable Receiver Circuit

The cable receiver circuit detects an input signal greater than nominal +.54v threshold. Output drive capability is 33 DTL unit loads. The receiver output signal is not inverted with respect to the input signal. As many as 25 cable receivers can be connected to the same cable because input current and capacitance are so low. All receivers connected to the cable are activated simultaneously by the signal on the cable.

LOGIC DIAGRAM, AJ10



SPECIFICATIONS, AJ10

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		10
Input (from cable)					
Logic 1 level	volts	front edge		2	
Logic 0 level	volts			0	
Permissible input range	volts		-1.5		4.4
Current per input*	μa				50
Input capacitance	pf				8
Switching threshold (adjustable)	volts		0.44	0.54	0.64
Output (to logic)					
Logic 1 level	volts	backplane pins	4.5		5.5
Logic 0 level	volts		0		0.4
Fan-out, into DTL	unit loads				33
Fan-out, into TTL					27
Propagation delay, at 25°C with load of 12.8 ma and 30 pf	ns			20	40
+5 volt supply	ma			165	440
+8 volt supply	ma			77	238
-8 volt supply	ma			81	252
Dissipation, per module	watts			2.1	6.6**

* Up to 25 receivers may be placed on one cable.
** At 5.5v

Long Lines

To use the AJ10, AJ11, or AJ12 with lines over 200 feet, employ the ET24 BNC Connector Tray and use 93-ohm coaxial cable in place of 33 ohm cable. (Reference: ET24 Module Data Sheet, Publication 901269). Only one long line can be driven by each driver; chaining is not allowed.

Mounting

An AJ10, AJ11, or AJ12 module requires only 1 module space provided that adjacent modules in the mounting case are not also cable drivers or receivers. Another type of module may be placed between each pair of AJ modules so that no space is wasted.

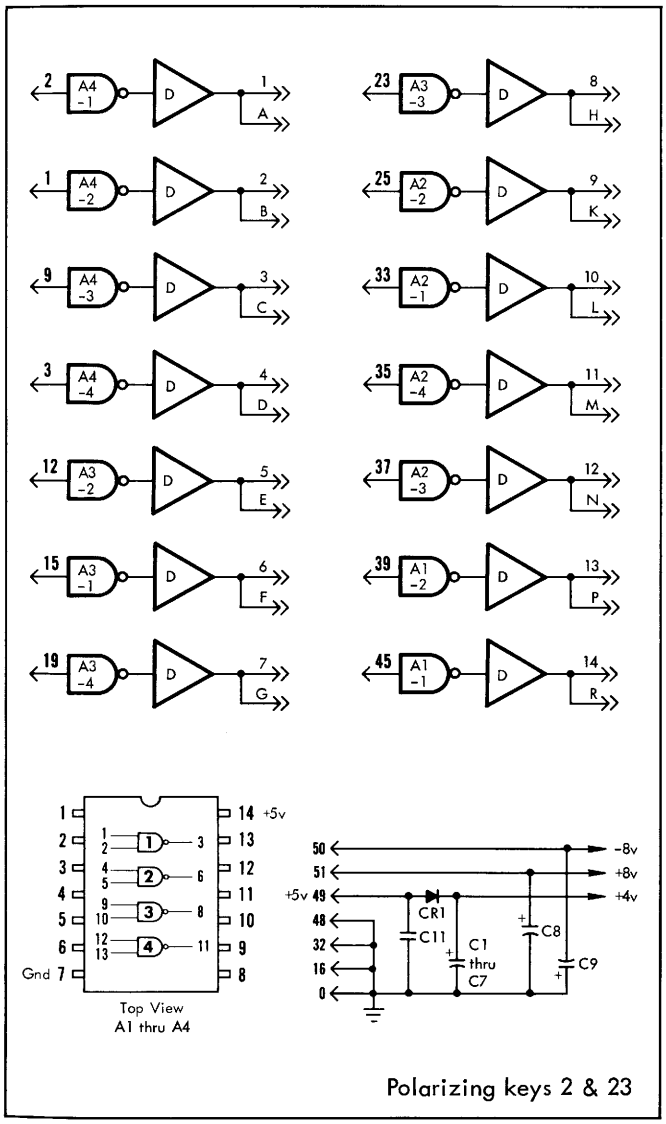
Grounding

In any system which uses cables between cabinets, the logic ground and power ground of all cabinets must be properly interconnected independently of the cable shield. Otherwise the cable shield acts as a ground return if it offers the lowest impedance path between the two separate ground systems. Noise pulses traveling down the shield between the two grounds can couple to the logic signal line and cause improper triggering at the receivers.

Schematics and Parts Lists

For complete schematic and parts list request AJ10/AJ11/AJ12 data sheet.

LOGIC DIAGRAM, AJ12



Polarizing keys 2 & 23

SPECIFICATIONS, AJ12

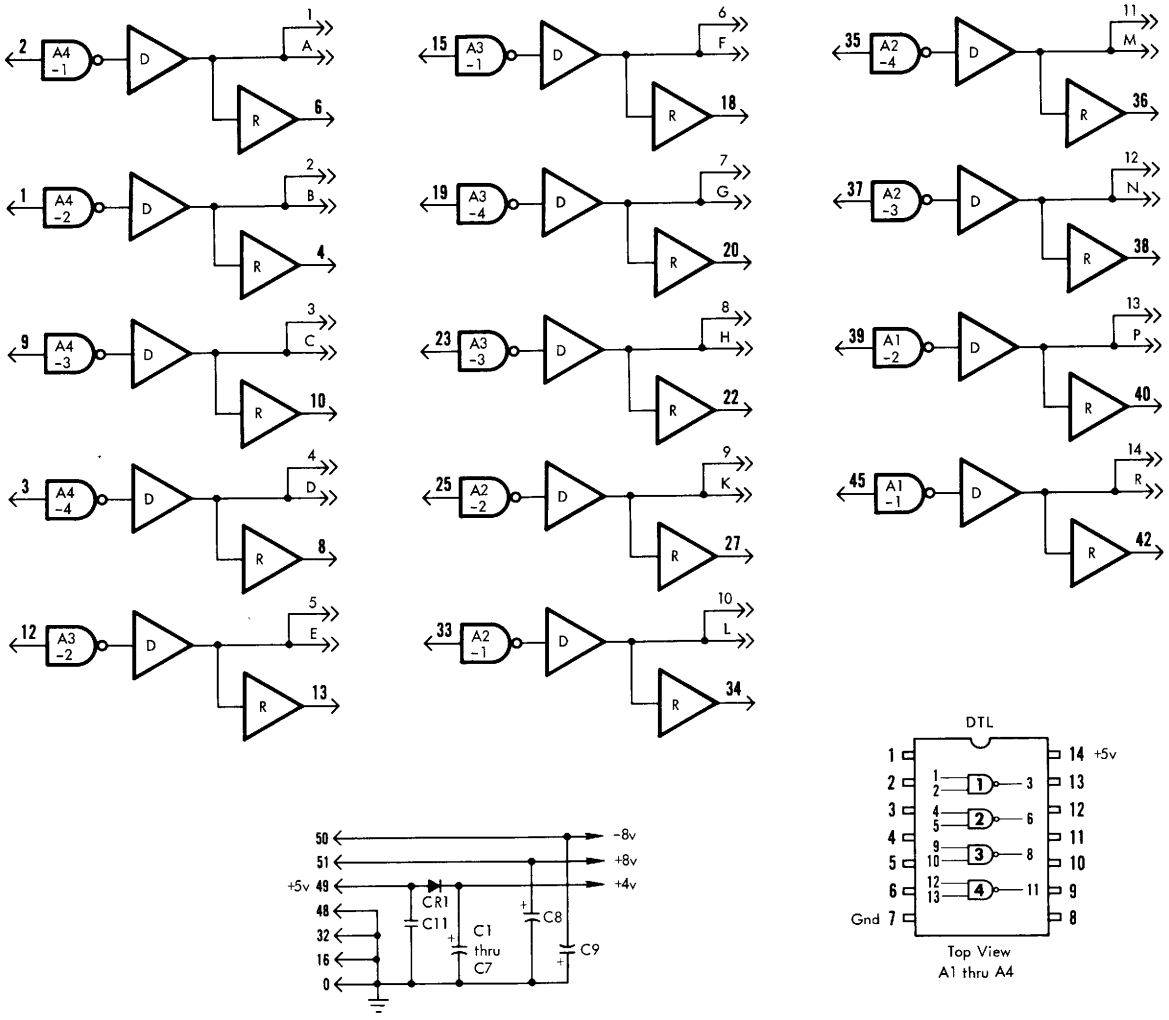
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Input level (from logic)		backplane pins			
Logic 1 level	volts		2.6		5.5
Logic 0 level	volts		0		0.4
Input loading	unit loads				1 DTL
Switching threshold	volts			1.5	
Output levels (to cable)		front edge			
Logic 1 level				2	
Logic 0 level				0	
Output loading	Output must be loaded with 16.5 ohms to ground, when used with 33 ohm cable (200 feet or less). Load should be two 33 ohm cables in parallel or one 33 ohm cable and a 33 ohm resistor to ground. ET13 dummy load has suitable resistors. When used with 93 ohm cable (up to 3,000 feet) use ET25 dummy load, which provides 93 ohm resistors. No chaining is allowed on long lines.				
Propagation delay at 25°C	ns			35	60
+5 volt supply	ma			878	1905
+8 volt supply	ma			195	315
Dissipation, per module	watts			5.9	10.7*

* at +5.5v

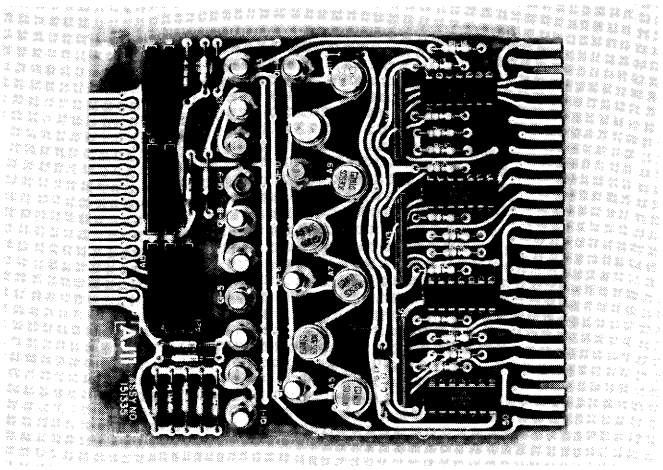
SPECIFICATIONS, AJ11

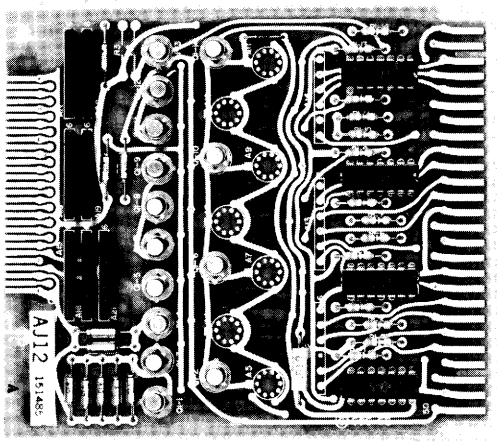
Performance specifications	Same as AJ10 for the receivers; same as AJ12 for the drivers
+5 volt supply	1043 ma typ., 2345 ma max.
+8 volt supply	272 ma typ., 553 ma max.
-8 volt supply	81 ma typ., 252 ma max.
Dissipation, per module	8.09 watts typ., 17.3 watts at +5.5v max.

LOGIC DIAGRAM, AJ11



Polarizing keys 2 & 23





AT22
SCHMITT TRIGGERS

The AT22 module contains two Schmitt Trigger circuits. Three input ranges are provided. Each Q output rises to +5v when input exceeds the adjustable trigger level, and returns to 0v when input drops below the adjustable hysteresis level, which is always more negative than the trigger level. Thus the trigger adjustment (R4) adjusts timing of the output leading edge while the hysteresis adjustment (R13) adjusts timing of the output trailing edge.

The Schmitt Trigger is needed to convert an input of arbitrary waveshape to a square wave which represents the two logic levels. It is often used to convert a sine wave to a square wave. It is also used as a pulse amplifier.

SPECIFICATIONS

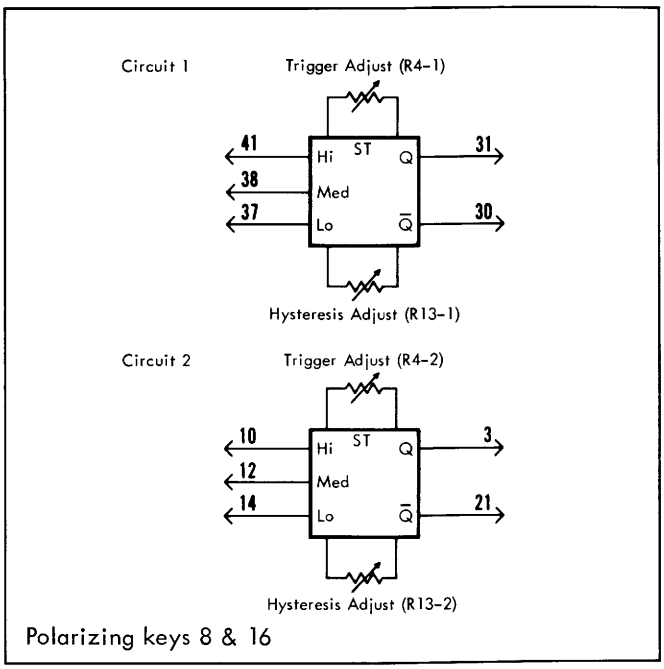
Characteristics	Units	Range	Min.	Typ.	Max.
Data rate	MHz		0		10
Input trigger levels (adjustable within the limits shown)	volts volts volts	low range med. range high range	-5 -15 -50		+ 5 +15 +50
Max. input voltage	3 times the input range shown above				
Input resolution	mv mv volts	low range med. range high range			± 50 ±150 ±0.5
Input threshold temp. coeff.	mv/°C				5
Input load to common	ohms	low range med. range high range		1K 3K 10K	
Output logic 1 level Output logic 0 level	volts volts		4.5 0		5.5 0.4
Fan-out, into DTL Fan-out, into TTL	unit loads				33 27
Propagation delay, at 25°C, with loads of 12.8 ma and 30 pf	ns			25	
+5 volt supply (Vcc) +8 volt supply -8 volt supply	ma ma ma			12 35 50	
Dissipation, per module	mw			740	814

A regulator on the module keeps thresholds stable. Outputs are fully buffered; a load on the output does not affect circuit operation.

Wire -8 volts from power supply to pin 50.

For complete schematic and parts list request AT22 data sheet.

LOGIC DIAGRAM



Polarizing keys 8 & 16

Table 1. Trigger and Hysteresis Ranges

Trigger (True Threshold)	Hysteresis
±5v	.5v to 1.5v
±15v	1.5v to 4.5v
±50v	4.0v to 17v

AT69
DIFFERENTIAL RECEIVERS

The AT69 module contains nine independent logic circuits with differential inputs (see connection diagram). When the voltage at the + input becomes at least 1 volt more positive than the voltage at the - input, and remains in that condition for at least 100 nsec, the output goes to logic 1 (high) level. It reaches this level 170 nsec after the input rising edge. When the differential between + and - inputs falls below 1 volt, the output falls 100 nsec later. An open circuit at the inputs also results in an output of logic 0 (low). Either a negative-going or positive-going signal is acceptable, since the circuit is sensitive only to the relative polarity of the input pair.

A differential receiver normally receives digital signals, over shielded cable or twisted-pair lines. A differential receiver has the advantage over a single-ended receiver that it rejects common-mode noise and ground potential differences. Common-mode voltages are those which appear between the two ends of a cable but are common to both of the input leads of the cable. With the AT69, a common mode rejection range of ±5 volts is provided when +8 volts and -8 volts are used as +V and -V. This rejection range can be increased to ±12 volts with ±V at ±15V.

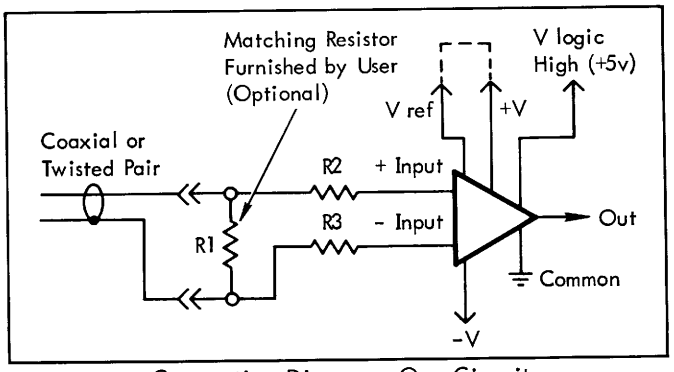
The maximum input data rate is 4 MHz. A filter network across the input terminals rejects all transients of up to 100 nsec duration, and should be removed when operating above 1 MHz. This filter furnishes an ac noise rejection which is in addition to the dc noise margin provided by the 1 volt threshold.

The optional resistor R1 (see connection diagram) functions as an impedance matching resistor for the input cable, and is provided by the user to match his particular cable impedance.

The AT69 output high logic level is determined by the supply voltage connected to pin 26, which for J Series use is +5v.

Both input terminals and the Vref terminal are available at front-edge cable connectors (⟶⟩) as well as back-panel connectors (⟶). The Vref terminal must be connected externally to +V as shown in the connection diagram. The circuit will not operate without the jumper.

The AT69 uses the same basic etched circuit board and most of the same circuit components as the HT73 Comparator Module.



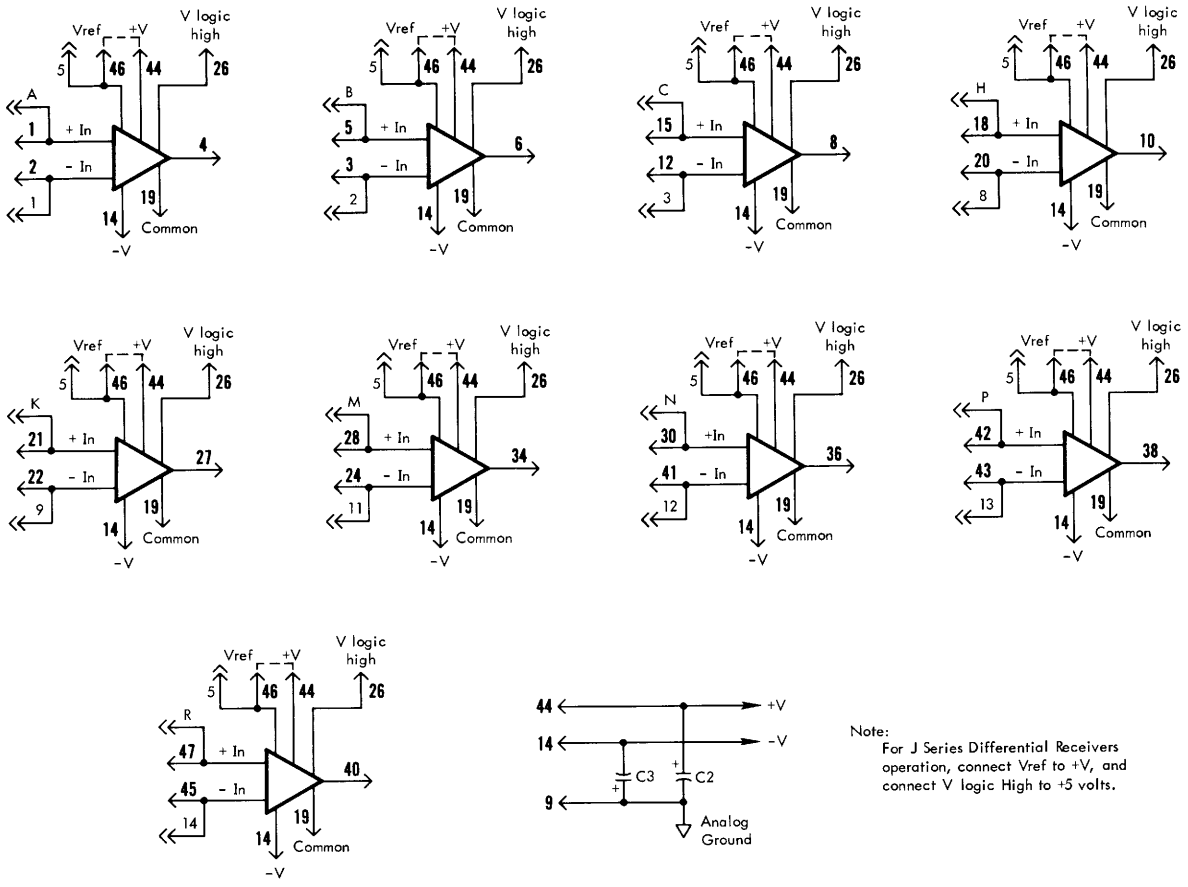
Connection Diagram, One Circuit

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Data rate	MHz		0		4
Differential threshold (at + input with respect to - input)	volts		0.8	1	1.2
Max. input voltage	volts				10
Input impedance (without R1)	ohms		200K		
Input pulsewidth (with filter in place)	ns		100		
Common mode rejection range (with ±8v at +V and -V)	volts		±5		
Common mode rejection range (with ±15v at +V and -V)	volts		±12v		
Output logic 1 level Output logic 0 level	volts volts		4.5 0		5.5 0.4
Fan-out, into DTL Fan-out, into TTL	unit loads	all outputs			37 30
Propagation delay, at 25°C: To rising edge of output To falling edge of output	 ns ns			 170 100	
+5 volt supply (Vcc) +8 volt supply -8 volt supply	ma ma ma			76 220 16	85 270 25
Dissipation, per module	watts			2.27	3.07*

* at 10% overvoltage

LOGIC DIAGRAM, AT69



Note:
For J Series Differential Receivers operation, connect Vref to +V, and connect V logic High to +5 volts.

Polarizing keys 3 & 13

BJ10
BCD TO 10-LINE DECODER (DTL)

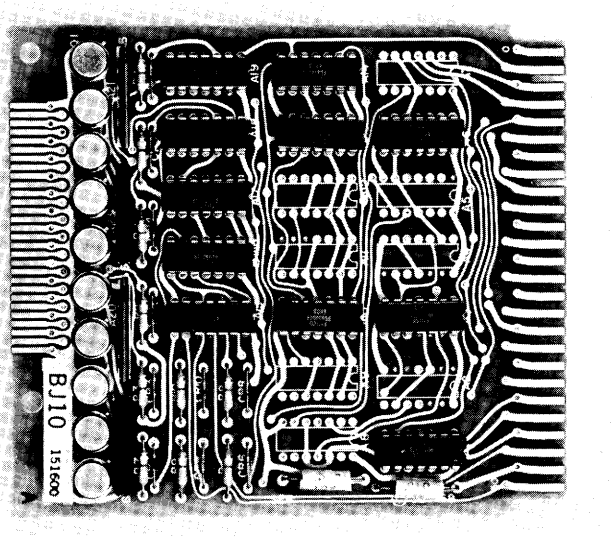
The BJ10 contains both a BCD to 10-line decoder and a group of ten indicator lamp (or relay) drivers. In addition, two independent 2-input NANDs are supplied on the module.

The decoder accepts a 4-bit binary-coded-decimal number, decides which one of ten outputs numbered 0 through 9 corresponds to the value of the BCD input, and generates a logic 0 on that output line. All nine other lines will be high (logic 1). An illegal input (10 through 15) results in all outputs being high (logic 1). The four BCD bits and their complements are required at the decoder input.

The ten driver inputs are connected directly to the ten decoder outputs. Each driver acts as a switch which is closed when its input is low. The drivers can also be used independently if decoder inputs are left open.

The BJ10 uses DTL circuits. The pin-compatible TTL version is BJ60.

The BJ10 uses the same general-purpose etch pattern that is used for BJ11, FJ16, and FJ17 modules. The board is partially filled with ICs to implement the desired logic function, as shown in the photograph at right.



PARTS LIST

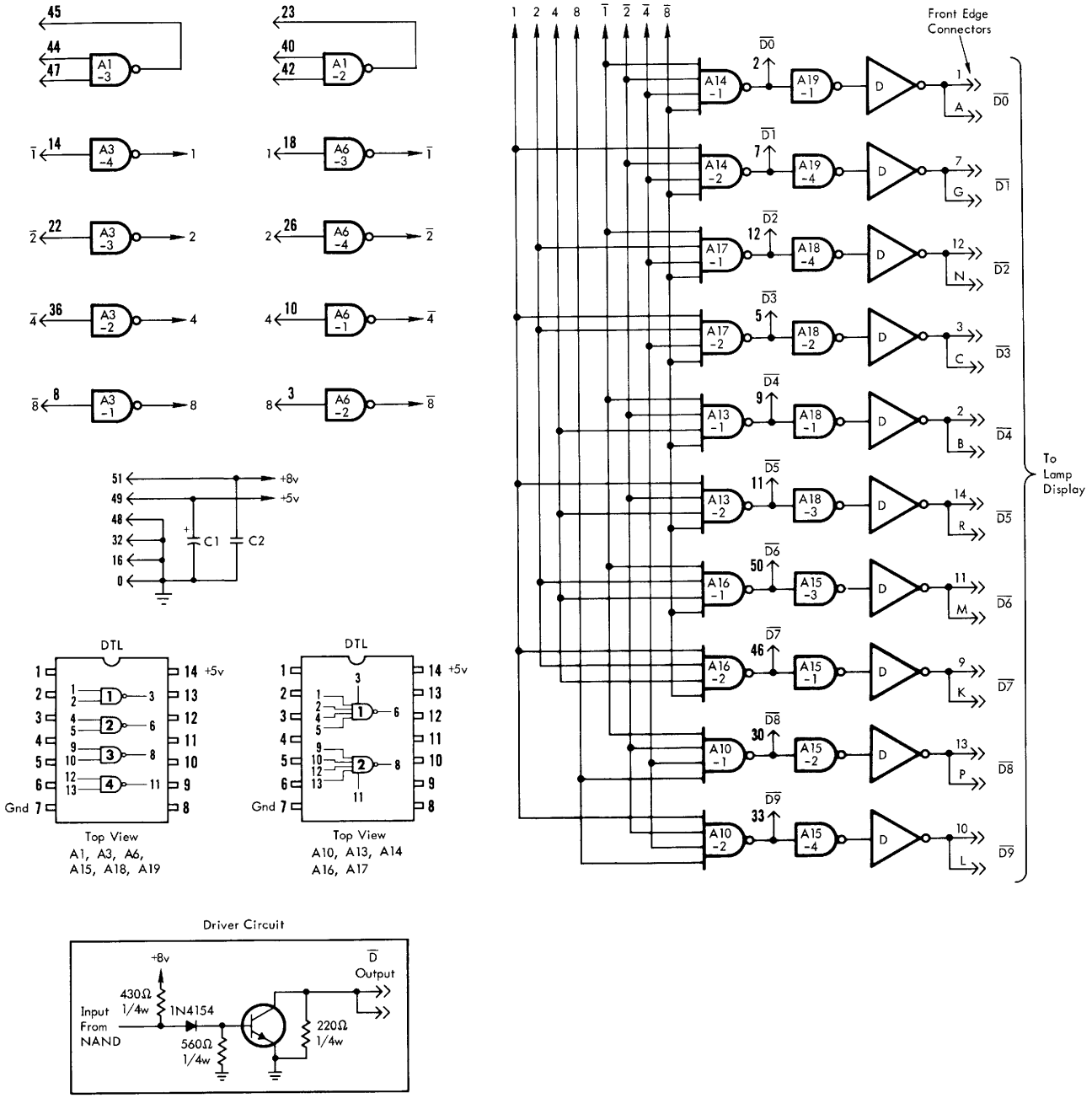
Designator	Description	Type	Qty.
A1, 3, 6, 15, 18, 19	IC gate, quad 2-in	946	6
A10, 13, 14, 16, 17	IC gate, dual 4-in	930	5
A20, 21	Res. network, 220Ω, 1/4w		2
A22, 23	Res. network, 560Ω, 1/4w		2
R1 thru 10	Res., 430Ω, 1/4w		10
CR1 thru 10	Diode	1N4154	10
Q1 thru 10	Transistor	2N3722	10
C1, 2	Cap., Mylar, .01μf		2

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL (at NAND outputs)	unit loads	2,7,12,5,9,11, 50,46,30, 33			7
Current per lamp driver (at 28vdc max.)	ma	front edge			200
Keep-alive resistor (designed for use with 5v bulb; remove if v exceeds 8v)	ohms watts			220 1/4	
Input loading	unit loads	14, 22, 36, 8, 18, 26, 10, 3			1
NAND propagation delay, at 25°C, with loads of 11.2 ma/30 pf	ns			60	100
+5 volt supply (Vcc) +8 volt supply	ma ma			54 198	76.6 216
Dissipation, per module	watts			1.86	2.33*

*at +5.5v

LOGIC DIAGRAM, BJ10



Polarizing keys 2 & 8

BJ11
BINARY TO 16-LINE DECODER (DTL)

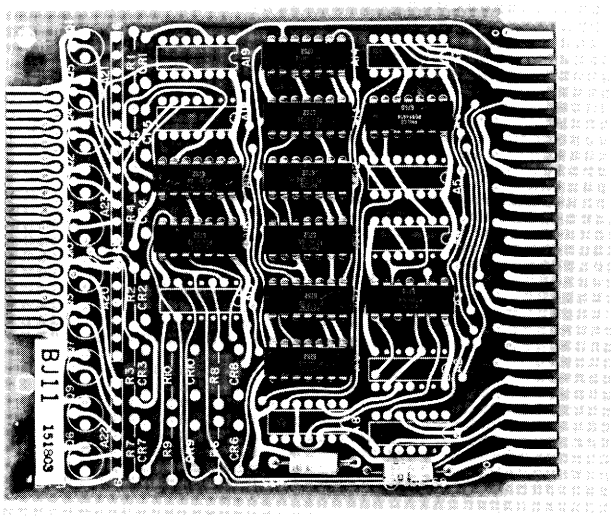
The BJ11 contains a binary input to 16-line output decoder.

A 4-bit binary input can assume any one of sixteen states. The BJ11 determines which one of these sixteen possible permutations of four bits is present at the inputs. It then generates a logic 0 (low) output on the one line whose assigned value (0 through 15) corresponds to the value of the 4-bit input. All of the other fifteen output lines will remain at logic 1 (high). Note that the outputs are given an inversion label (overscore) to indicate that a logic 0 represents the desired condition. Refer to the block diagram, below.

The input to the module requires eight signals. Both logic phases (signal and complement) of each of the four input bits is required.

The BJ11 uses DTL circuits. The pin-compatible TTL version is BJ61.

The BJ11 uses the same general-purpose etch pattern that is used for the BJ10, FJ16, and FJ17 modules. This board is only partially filled with ICs, as shown in the photo below, to implement the desired logic function.

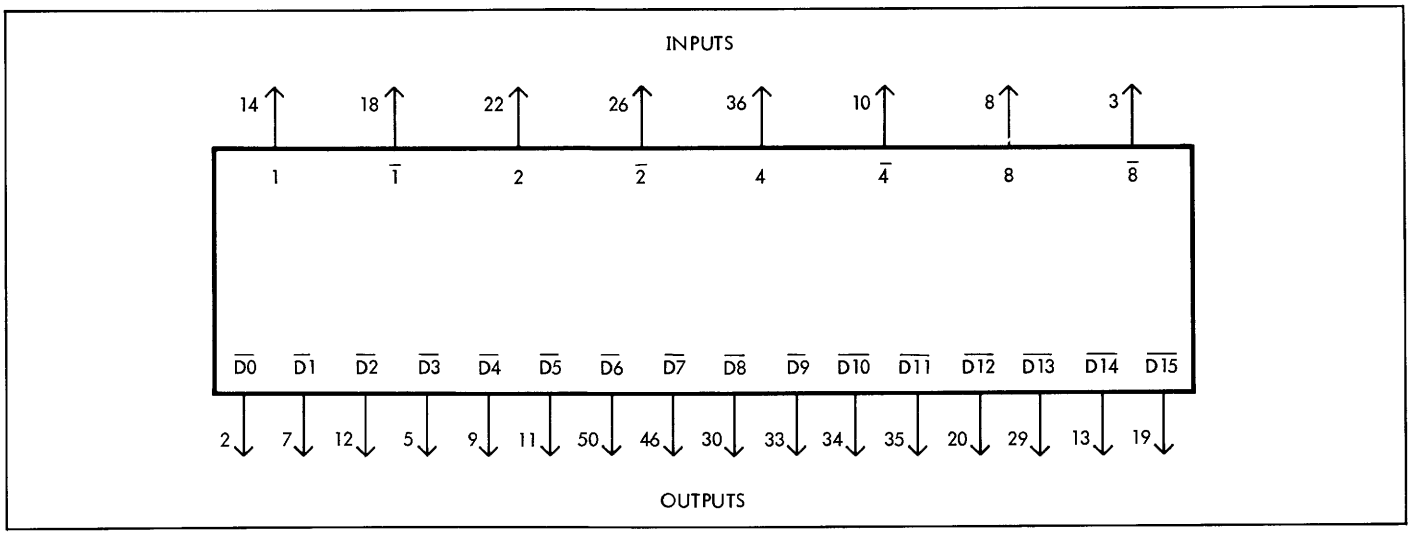


SPECIFICATIONS

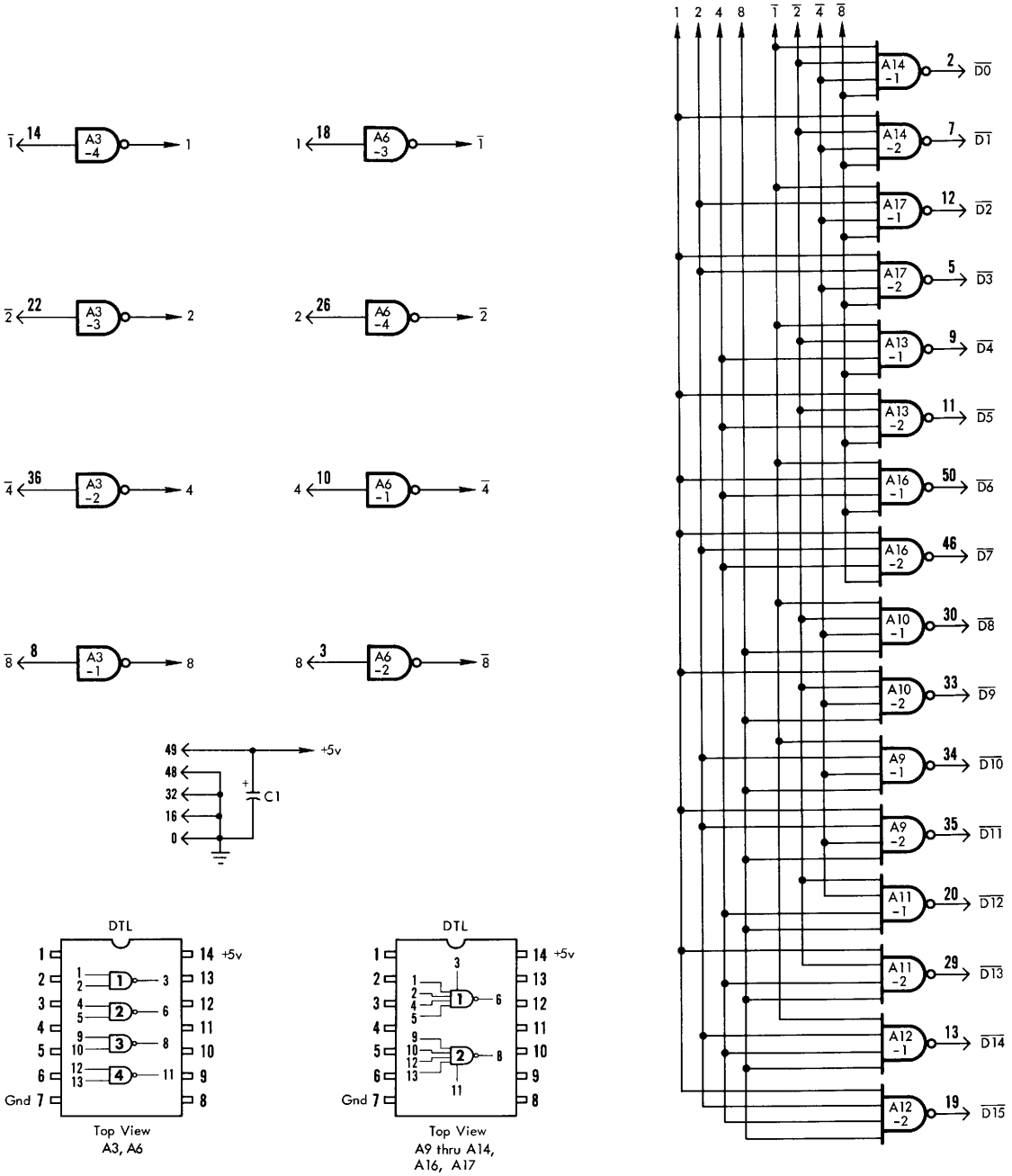
Characteristics	Units	Pin No's	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			60	100
+5 volt supply (Vcc) (max ma are at +5.5v)	ma			46.8	65.6
Dissipation, per module	mw			234	361

PARTS LIST

Designator	Description	Type	Qty.
A3, 6	IC gate, quad 2-in	946	2
A9, 10, 11, 12, 13, 14, 16, 17	IC gate, dual 4-in	930	8
C1, 2	Cap. mylar .01μf		2



LOGIC DIAGRAM, BJ11



Polarizing keys 2 & 8

BJ12
BCD TO 10-LINE DECODERS (DTL)

The BJ12 contains three independent decades of decoding, each with BCD input and 10-line output.

A 4-bit Binary-Coded-Decimal number can assume any one of ten distinct states. The BCD/10-line decoder determines which one of these ten possible permutations of four bits is present at the inputs. It then generates a logic 0 (low) output on the one line whose assigned value (0 through 9) corresponds to the value of the 4-bit input. All of the other nine output lines will remain at logic 1 (high). Note that the outputs are given an inversion label (overscore) to indicate that a logic 0 represents the desired condition. Refer to the block diagram, below.

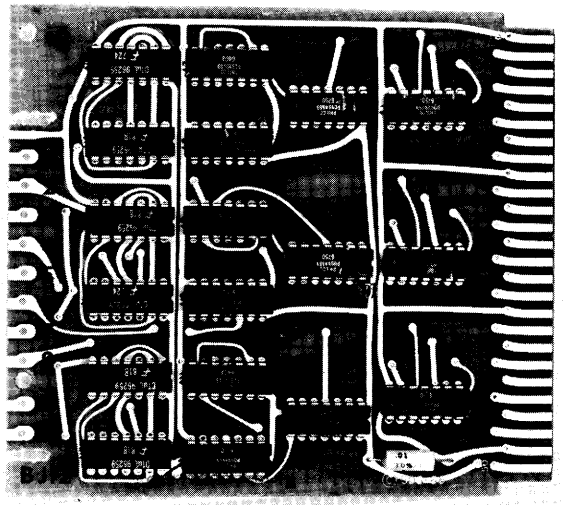
An illegal input (a 4-bit input representing one of the values 10 through 16) will cause all ten outputs to go high.

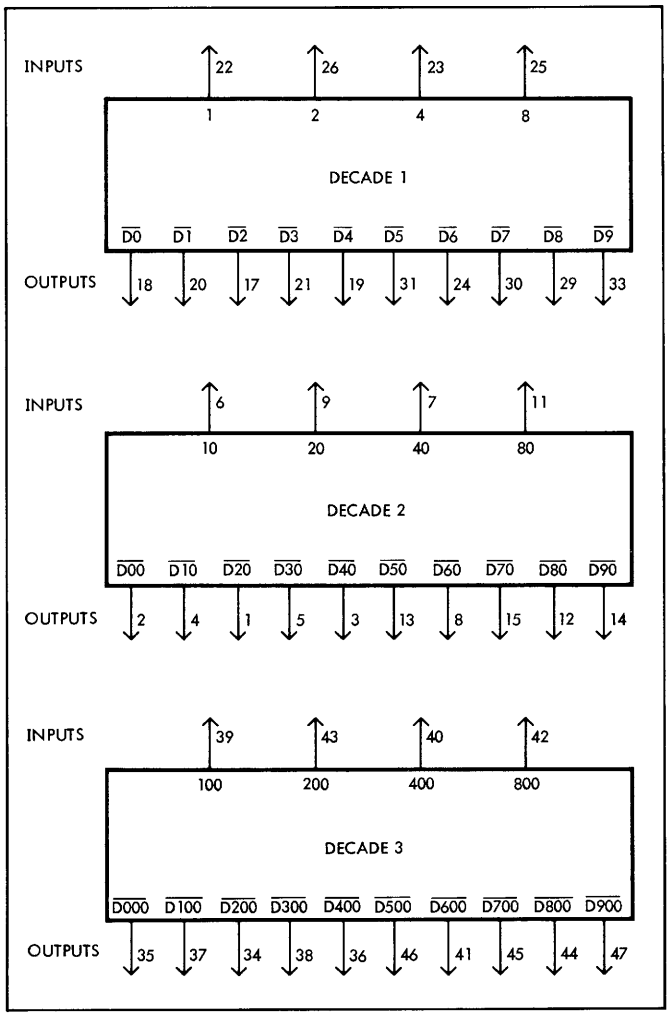
The input to each decade decoder requires only four signals. Complements are generated on the module.

The BJ12 uses DTL circuits. The pin compatible TTL version is BJ62.

Test points are provided on one of the three decades.

This module will conveniently interface with the FJ18.





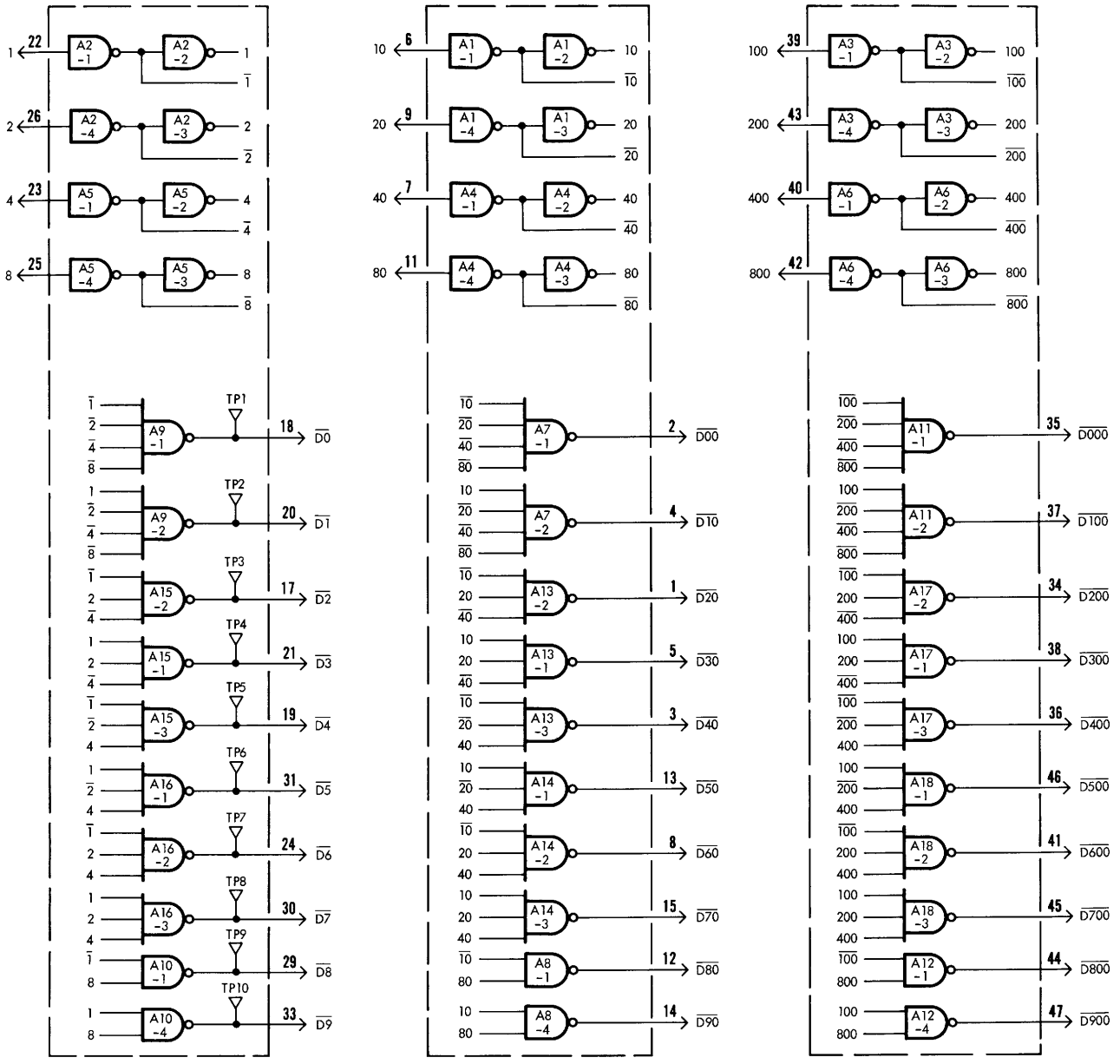
SPECIFICATIONS

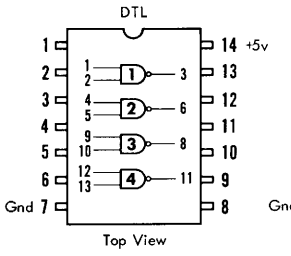
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			90	150
+5 volt supply (Vcc) (max ma at +5.5v)	ma			86.4	120.6
Dissipation, per module	mw			432	665

PARTS LIST

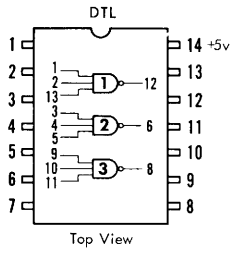
Designator	Description	IC Type	Qty.
A1 thru 6, A8, 10, 12	IC gate, quad 2-in	946	9
A7, 9, 11	IC gate, dual 4-in	930	3
A13 thru 18	IC gate, triple 3-in	962	6
C1, 2	Cap. mylar, .01μf		2

LOGIC DIAGRAM, BJ12

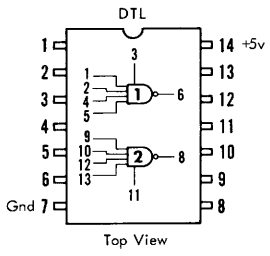




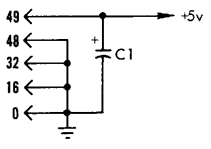
A1 thru A6,
A8, A10, A12



A13 thru A18



A7, A9, A11



Polarizing keys 3 & 7

BJ60.
BCD TO 10-LINE DECODER (TTL)

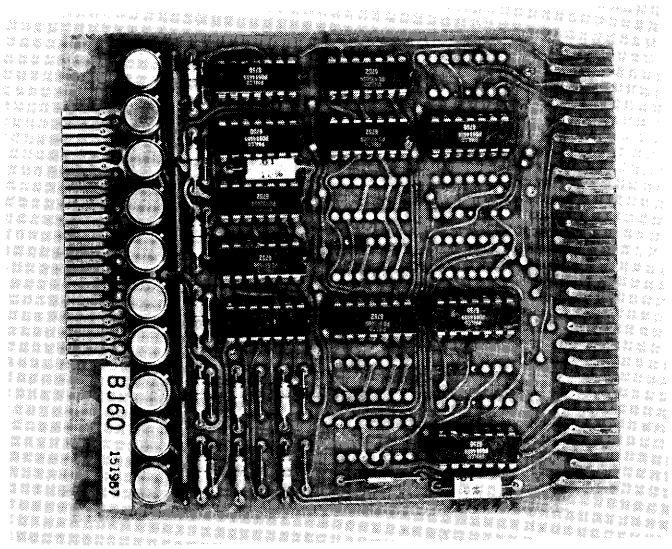
The BJ60 contains both a BCD to 10-line decoder and a group of ten indicator lamp (or relay) drivers. In addition, two independent 2-input NANDs are supplied on the module.

The decoder accepts a 4-bit binary-coded-decimal number, decides which one of ten outputs numbered 0 through 9 corresponds to the value of the BCD input, and generates a logic 0 on that output line. All other nine lines will be high (logic 1). An illegal input (10 through 15) results in all outputs being high (logic 1). The four BCD bits and their complements are required at decoder input.

The ten driver inputs are connected directly to the ten decoder outputs. Each driver acts as a switch which is closed when its input is low.

The BJ60 uses TTL circuits. The pin-compatible DTL version is BJ10.

The BJ60 uses the same general-purpose etch pattern as the BJ61, FJ66, and FJ67 modules, partially filled with ICs to implement the desired logic function, as shown in the photograph at right.



PARTS LIST

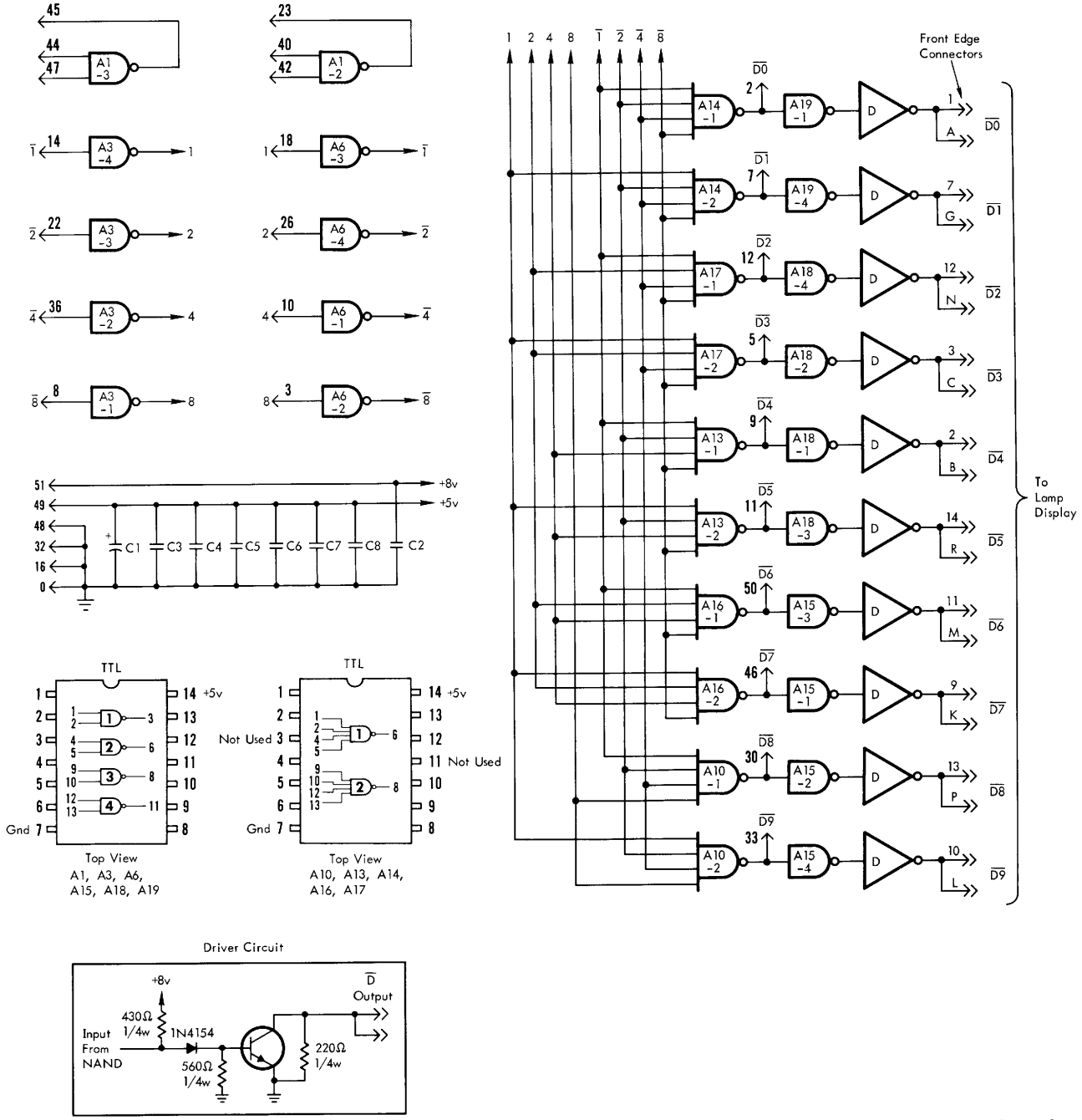
Designator	Description	Type	Qty.
A1, 3, 6, 15, 18, 19	IC gate, quad 2-in	9002	6
A10, 13, 14 16, 17	IC gate, dual 4-in	9004	5
A20, 21	Res. network, 220Ω, 1/4w		2
A22, 23	Res. network, 560Ω, 1/4w		2
R1 thru 10	Res., 430Ω, 1/4w		10
CR1 thru 10	Diode	1N4154	10
Q1 thru 10	Transistor	2N3722	10
C2 thru 8	Cap., Mylar, .01μf		7
C1	Cap., Tantalum, 1μf		1

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL (at NAND outputs)	unit loads	2,7,12,5,9,11, 50,46,30,33			7
Current per lamp driver (at 28vdc max)	ma	front edge			200
Keep-alive resistor (designed for use with 5V bulb; remove if V exceeds 8V)	ohms watts			220 1/4	
Input loading	unit loads	14, 22, 36, 8, 18, 26, 10, 3			1
NAND propagation delay, at 25°C, with loads of 15pf	ns			20	28
+5 volt supply (Vcc) +8 volt supply	ma ma			63 198	330* 216
Dissipation, per module	watts			3.49	5.63*

*at +5.5v and 20 MHz

LOGIC DIAGRAM, BJ60



Polarizing keys 2 & 8

BJ61
BINARY TO 16-LINE DECODER (TTL)

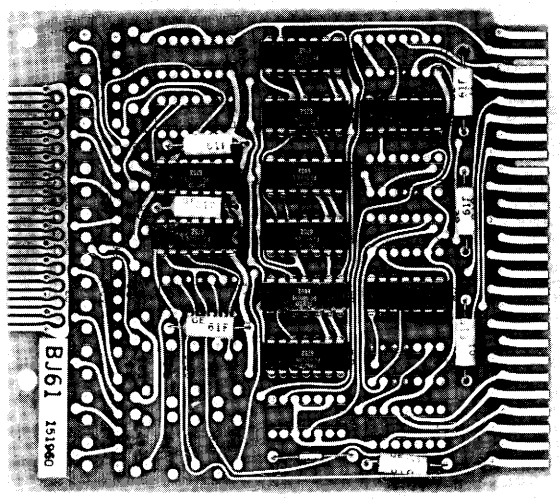
The BJ61 contains a binary input to 16-line output decoder.

A 4-bit binary input can assume any one of sixteen states. The BJ61 determines which one of these sixteen possible permutations of four bits is present at the inputs. It then generates a logic 0 (low) output on the one line whose assigned value (0 through 15) corresponds to the value of the 4-bit input. All of the other fifteen output lines will remain at logic 1 (high). Note that the outputs are given an inversion label (overscore) to indicate that a logic 0 represents the desired condition. Refer to the block diagram, below.

The input to the module requires eight signals. Both logic phases (signal and complement) of each of the four input bits is required.

The BJ61 uses TTL circuits. The pin-compatible DTL version is BJ11.

The BJ61 uses the same general-purpose etch pattern that is used for the BJ60, FJ66, and FJ67 modules. This board is only partially filled with ICs, as shown in the photo below, to implement the desired logic function.



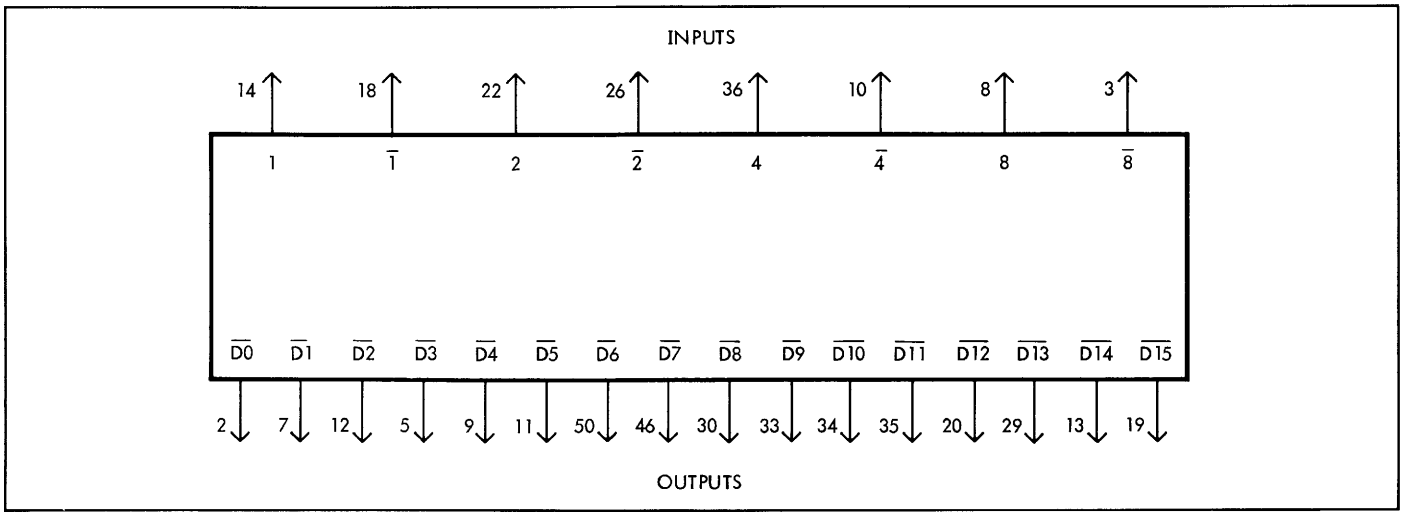
SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	All outputs			8
Input loading	unit loads	All inputs			1
Propagation delay, at 25°C, with loads of 15pf	ns			20	28
+5 volt supply (Vcc)	ma			46.8	286*
Dissipation, per module	mw			234	1,570*

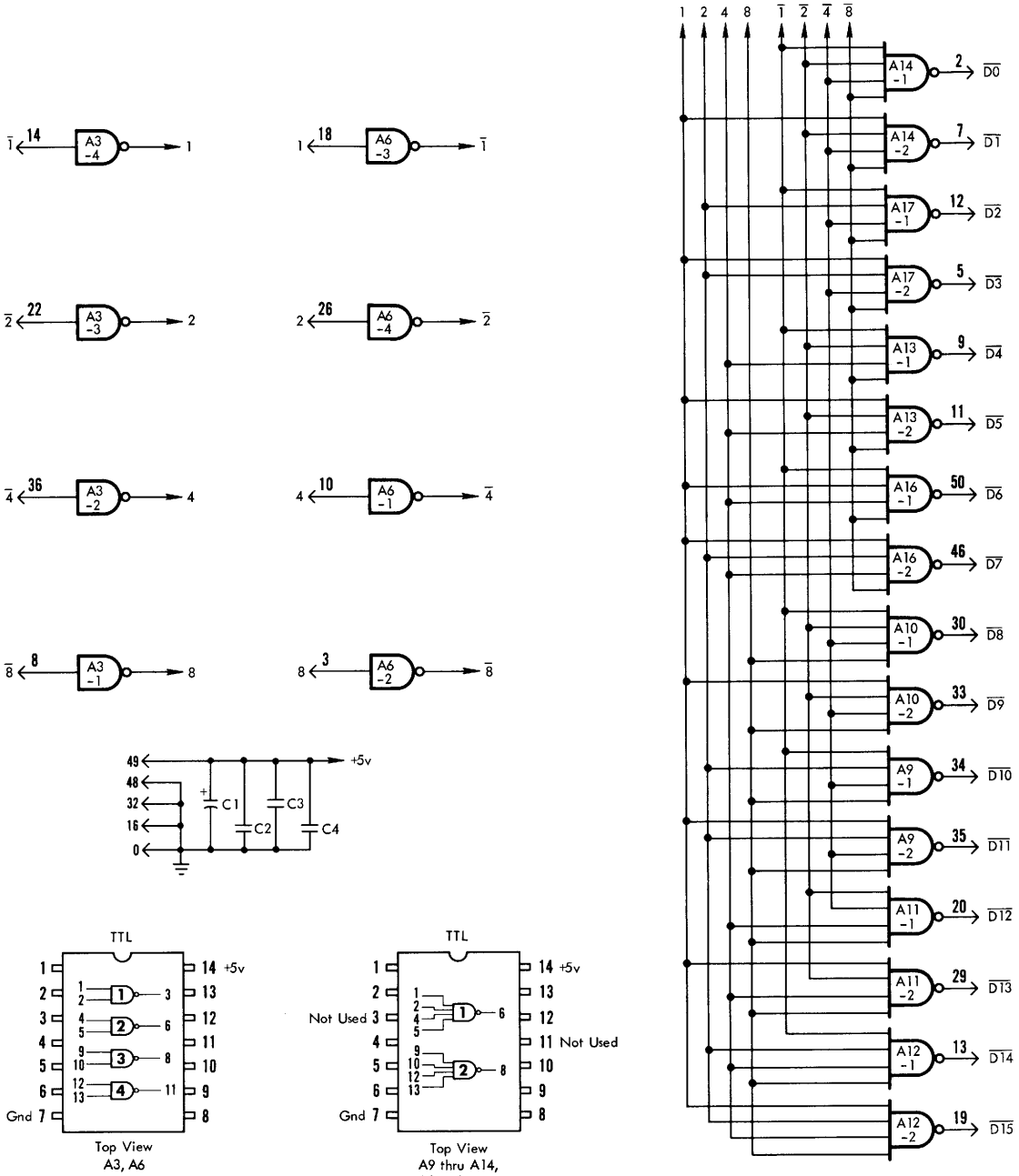
* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	Type	Qty.
A3, 6	IC gate, quad 2-in	9002	2
A9, 10, 11, 12, 13, 14, 16, 17	IC gate, dual 4-in	9004	8
C2 thru 8	Cap., mylar, .01μf		7
C1	Cap., tantalum, 1μf		1



LOGIC DIAGRAM, BJ61



Polarizing keys 2 & 8

BJ62
BCD TO 10-LINE DECODERS (TTL)

The BJ62 contains three independent decades of decoding, each with BCD input and 10-line output.

A 4-bit Binary-Coded-Decimal number can assume any one of ten distinct states. The BCD/10-line decoder determines which one of these ten possible permutations of four bits is present at the inputs. It then generates a logic 0 (low) output on the one line whose assigned value (0 through 9) corresponds to the value of the 4-bit input. All of the other nine output lines will remain at logic 1 (high). Note that the outputs are given an inversion label (overscore) to indicate that a logic 0 represents the desired condition. Refer to the block diagram, below.

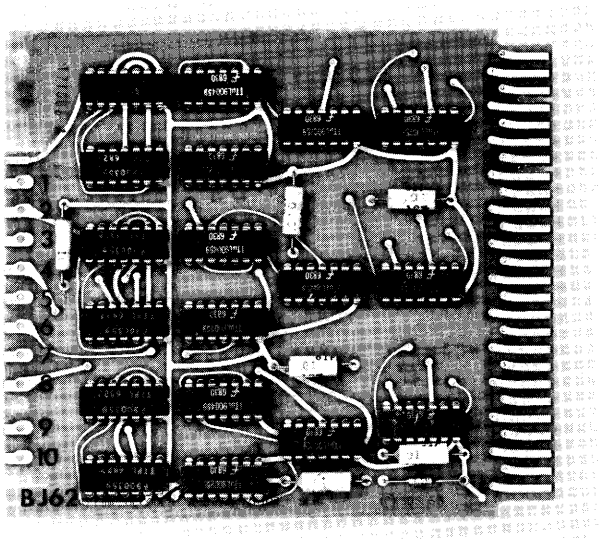
An illegal input (a 4-bit input representing one of the values 10 through 16) will cause all ten outputs to go high.

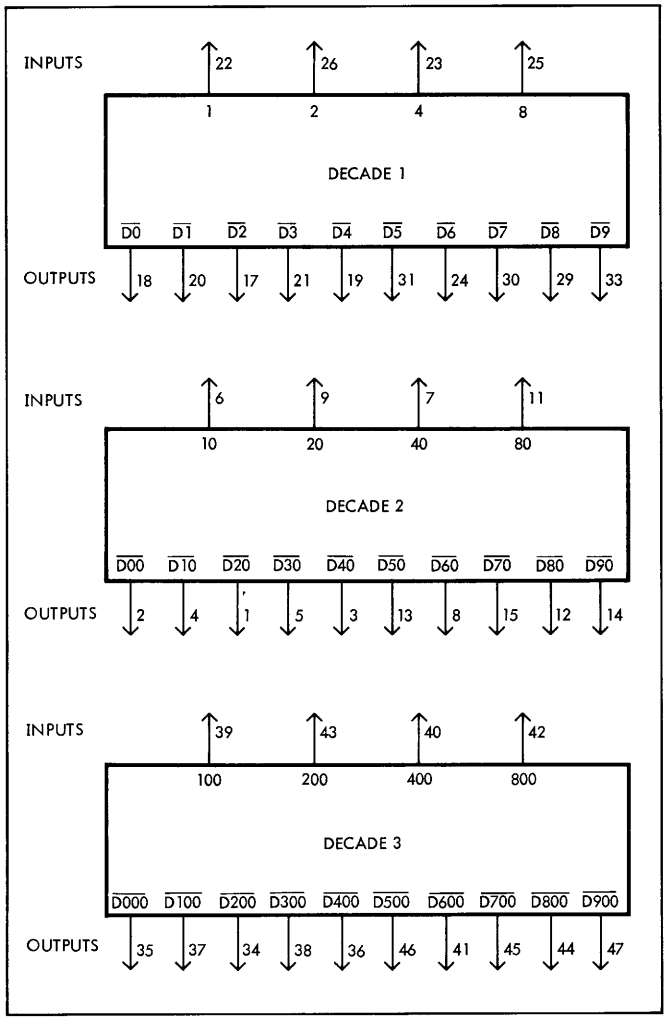
The input to each decade decoder requires only four signals. Complements are generated on the module.

The BJ62 uses TTL circuits. The pin compatible DTL version is BJ11.

Test points are provided on one of the three decades.

This module will conveniently interface with FJ68.





SPECIFICATIONS

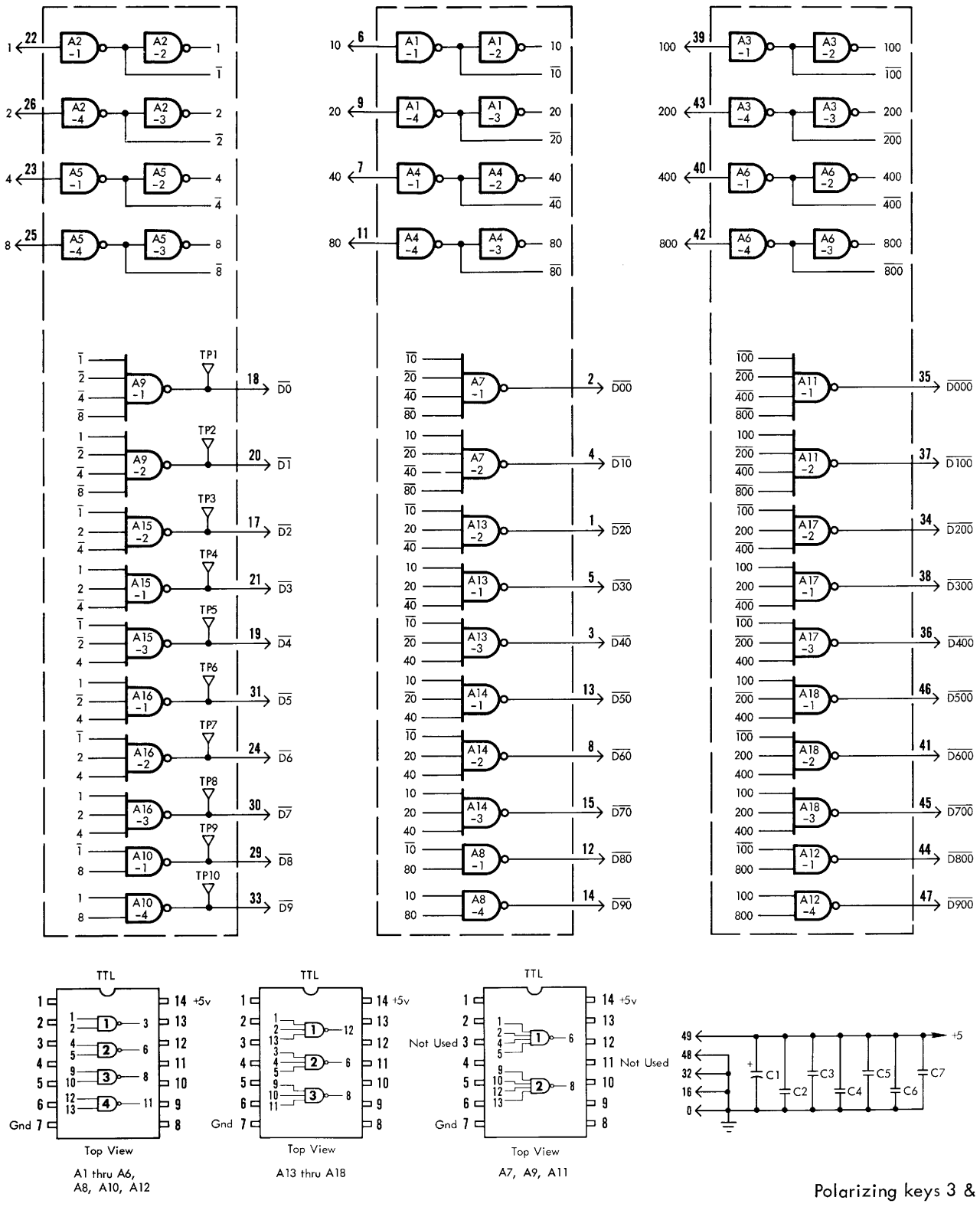
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	All outputs			8
Input loading	unit loads	All inputs			1
Propagation delay, at 25°C, with loads of 15pf	ns			30	42
+5 volt supply (Vcc)	ma			86.4	528*
Dissipation, per module	mw			432	2,900*

*at +5.5v and 20 MHz

PARTS LIST

Designator	Description	Type	Qty.
A1 thru A6, A8, A10, A12		9002	9
A7, A9, A11		9004	3
A13 thru A18		9003	6
C2 thru C7	Cap., Mylar, .01μf		6
C1	Cap., Tantalum, 1μf		1

LOGIC DIAGRAM, BJ62



CJ16
MEDIUM FREQUENCY CLOCK OSCILLATOR

The CJ16 module contains a 1 MHz to 2 MHz oscillator with 50% duty cycle squarewave output, and a seven stage downcounter. Oscillator is controlled by LC or crystal. When crystal control is desired frequency must be specified by the user. For higher output drive capability feed output through logic driver before connecting to clock line.

Clock can be bussed via ordinary logic wiring. Terminate clock bus with one 1.1K ohm resistor on XJ10 module. Lines should radiate from driver in equal lengths to avoid clock skew.

If more than one frequency is employed in the system, the phase shift due to delay through the seven-stage ripple counter should be taken into account.

Wire -8 volts from power supply to pin 50. Other supply voltages are provided on back panel etch. When using crystal, adjust frequency to correct value with LC control before plugging in crystal. Have LC jumper in place when adjusting LC control. Remove LC jumper and insert crystal jumper before placing crystal in circuit. Then tweak LC control for maximum output at crystal frequency.

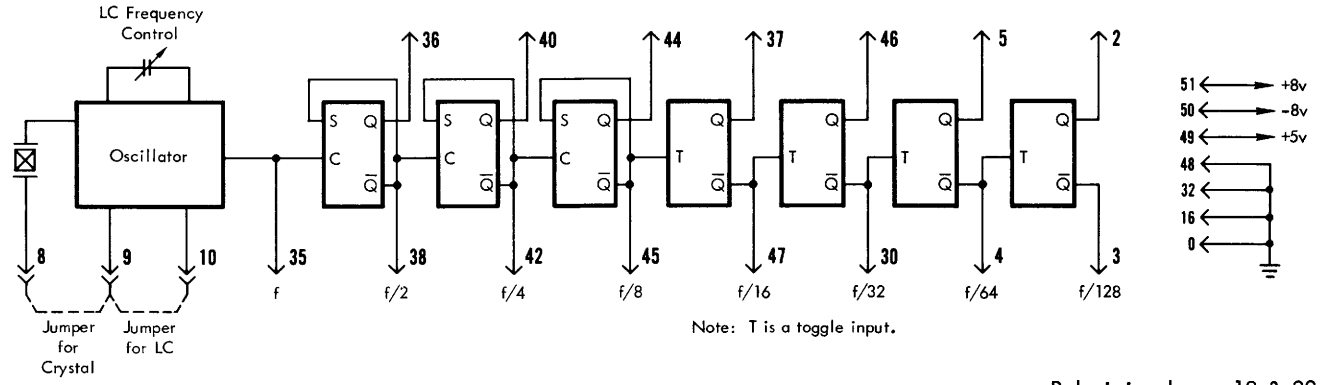
To obtain a detailed circuit schematic and parts list, request a CJ16 data sheet.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	KHz MHz		7.8		 2
Stability, crystal operation	ppm/°C		2		
Crystal freq. accuracy	%		±0.02		
Logic 1 level Logic 0 level	volts volts		4.5 0		5.5 0.4
Fan-out	unit loads				
Into DTL		36, 40, 44 35 38, 42, 45 all others			33 31 30 23
Into TTL		36, 40, 44 35 38, 42, 45 all others			27 27 27 25
+5 volt supply*	ma			216	240†
+8 volt supply*	ma			77	85†
-8 volt supply*	ma			47	52†
Dissipation, per module	watts			2.1	2.3†

* based on 50% duty cycle
† at +5.5v

LOGIC DIAGRAM



Note: T is a toggle input.

Polarizing keys 18 & 22

CT10
HIGH FREQUENCY CLOCK OSCILLATOR

The CT10 contains a 1 MHz to 10 MHz oscillator, a pulse shaper, and a gated clock amplifier (driver). The oscillator is controlled by an adjustable LC circuit or optionally by a plug-in crystal. External jumpers select range (see table 1). When crystal control is desired frequency must be specified by the user. When using crystal, first adjust to approximate frequency using LC control with jumper 45-20 in place. Then remove jumper 45-20 and insert crystal.

Table 1. Frequency Ranges

Frequency Range	Jumper
6.20 to 10 MHz	none
3.90 to 6.30 MHz	39, 44
2.48 to 4.00 MHz	40, 44
1.56 to 2.53 MHz	40, 41, 44
1.0 to 1.59 MHz	40, 42, 44

Pulsewidth control on shaper adjusts duty cycle from approximately 30% to approximately 70%. This adjustment is frequency dependent and should be checked with an oscilloscope.

Clock can be bussed via ordinary logic wiring. Terminate clock bus with one or more 1.1K ohm resistors on an XJ10 module. Lines should radiate from driver in equal lengths to avoid clock skew.

Since the driver gate is an AND/OR gate each unused OR input must be grounded, by grounding one AND term of the AND gate which precedes the OR term. For instance, if the gate 26-27-29 is not used, ground one of the three pins 26, 27, or 29.

Wire -8 volts from power supply to pin 50.

This module requires two card slots.

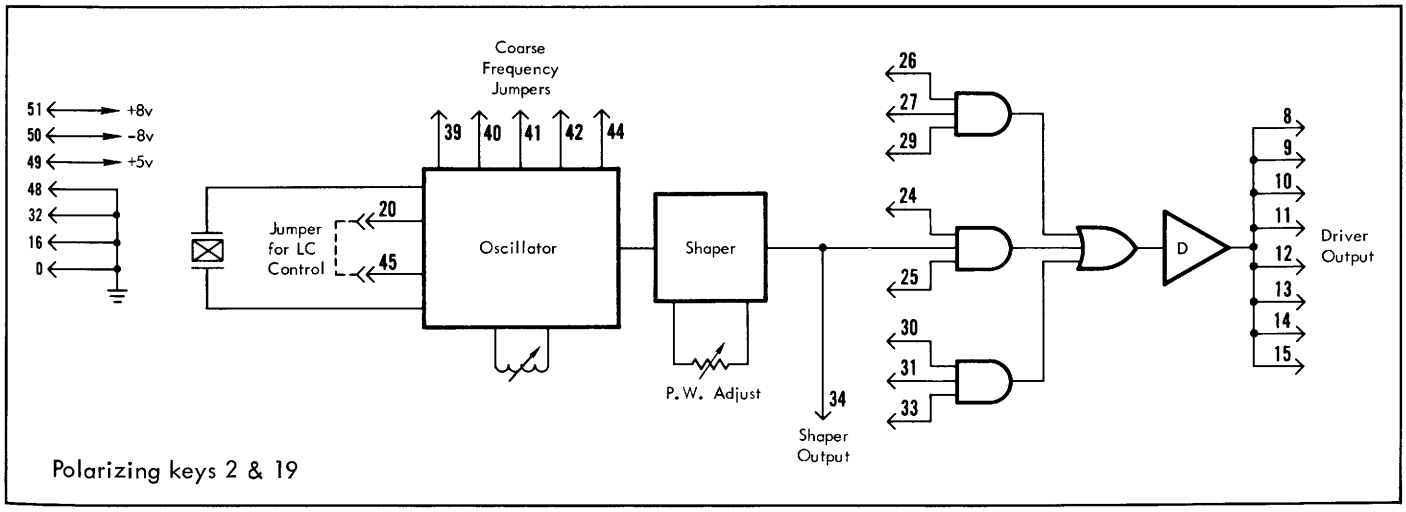
To obtain a detailed circuit schematic and parts list, request a CT10 data sheet.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		1		10
Stability, crystal operation	ppm/°C		2		
Crystal freq. accuracy	%		±0.02		
Logic 1 level Logic 0 level	volts volts		4.5 0		5.5 0.4
Fan-out from driver Into DTL Into TTL	 unit loads	 8 thru 15			 174 131
Fan-out from shaper Into DTL Into TTL	 unit loads	 34			 16 16
Input loading at driver control gate (each input, from either DTL or TTL)	unit loads				5
+5 volt supply*	ma			44	48†
+8 volt supply*	ma			117	130†
-8 volt supply*	ma			54	60†
Dissipation, per module	watts			1.59	1.76†

* based on 50% duty cycle
† at +5.5v

LOGIC DIAGRAM



DJ24
9-BIT AND SIGN D/A CONVERTER

The DJ24 is a high accuracy 9-bit and sign digital-to-analog converter with ±4 ma or ±10 volts (±20 ma) bipolar output. The module includes a resistive ladder network, switches and drivers, and an output amplifier. It accepts 2's complement values of input code to produce a negative output. It can be recalibrated to accept 1's complement input.

A digital register such as the FJ20 module can be used to store the digital input.

Either voltage or current output is available, both with 0.1% maximum error referred to reference source, over the full temperature range. The voltage output is obtained by feeding the current output into an IC operational amplifier, provided on the board, which has a full scale output of ±10v and can drive a 20ma resistive load with 5,000 pf of parallel capacitance.

Input logic levels are standard J Series, 1 unit load per input. The WT49 regulator module is available to provide ±35 volts reference source. Wire the reference voltages and -8v to pins shown in the input-output diagram.

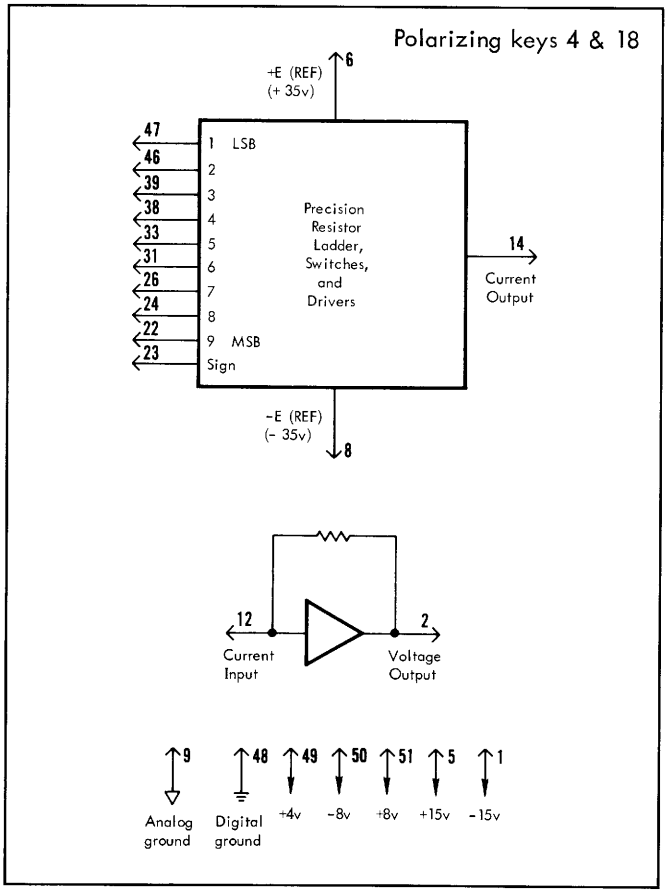
The output voltage is related to digital input as shown in Table 1.

To obtain detailed circuit schematic and parts list, request a DJ24 data sheet.

Table 1. Input vs Output Relations

DIGITAL INPUT				ANALOG OUTPUT VOLTAGE			
Sign Bit	MSB	2^{-2} ... 2^{-8}	LSB	2's Complement		1's Complement	
0	0	1 1 1 1 1 1 1	1	$FS-\frac{FS}{2^9}$	$9\frac{502}{512}$ v	$FS-\frac{FS}{2^9}$	$9\frac{502}{512}$ v
0	0	0 0 0 0 0 0 0	1	$\frac{FS}{2^9}$	$\frac{10}{512}$ v	$\frac{FS}{2^9}$	$\frac{10}{512}$ v
0	0	0 0 0 0 0 0 0	0	0	0v	+0	+0v
1	1	1 1 1 1 1 1 1	1	$-\frac{FS}{2^9}$	$-\frac{10}{512}$ v	-0	-0v
1	1	1 1 1 1 1 1 1	0	$-\frac{FS}{2^8}$	$-\frac{10}{256}$ v	$-\frac{FS}{2^9}$	$-\frac{10}{512}$ v
1	0	0 0 0 0 0 0 0	0	-FS	- 10 v	$-FS+\frac{FS}{2^9}$	$-9\frac{502}{512}$ v

INPUT-OUTPUT DIAGRAM

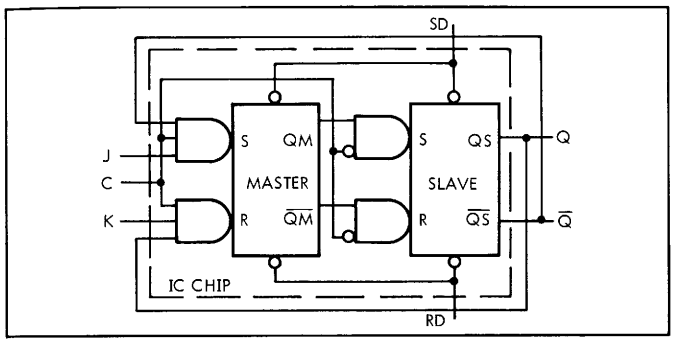


SPECIFICATIONS

Characteristic	Units	Min.	Typ.	Max.
Overall characteristics				
Resolution (including sign)	bits			10
Accuracy (relative to ref. voltage)	%	0.1		
Temperature range	°C	0		+55
Output characteristics				
Voltage output range, full scale (Op. amp.)	volts	-10		+10
Voltage output conversion time to reach within 10mv of final value (add items 1 and 2):				
1. Settling time	μsec			5
2. Slewing time per volt of output change	μsec/v			2.6
Current output range, full scale				
1. without Op. Amp.	ma	-4		+4
2. from Op. Amp.	ma	-20		+20
Current output switching time (for a transition from - full scale current to - full scale current)	nsec			<100
Input characteristics				
Logic 1 level	volts	2.6		5.5
Logic 0 level	volts	0		0.4
Switching threshold	volts		1.5	
Input loading	unit loads			1
Power requirements				
-5 volt supply	ma			75
+8 volt supply	ma			73
-8 volt supply	ma			25
+15 volt supply	ma			36
-15 volt supply	ma			36
+35 volt supply	ma			10.5
-35 volt supply	ma			7.5
Dissipation, per module	watts			2.2

The FJ10 module contains eight JK flip-flops (RS flip-flops connected via etch in the JK mode), with two common Reset Direct (clear) lines. One group of four also has individual Set Direct inputs.

Each JK flip-flop is a clocked storage element consisting of a master and a slave flip-flop placed on the same IC chip, functionally related as shown in the diagram below. The master-slave principle has the advantage that the circuit is not sensitive to rise or fall times of clock signals, or to clock pulsewidth, providing that the pulsewidth exceeds the minimum required for internal propagation delays. The clock signal, when high, moves J or K input data into the master flip-flop; when it goes low it causes data to transfer from master to slave. The clock input is shown with an inversion symbol to indicate that data appears at the outputs when clock goes low.



The FJ10 Set Direct (SD) and Reset Direct (RD) inputs override the clocked (J and K) inputs. A low level (0v) is used to activate SD or RD.

Truth table is given at the beginning of this section, under the heading "Logic Symbols".

The FJ10 uses DTL circuits. Refer to FJ60 for TTL version.

PARTS LIST

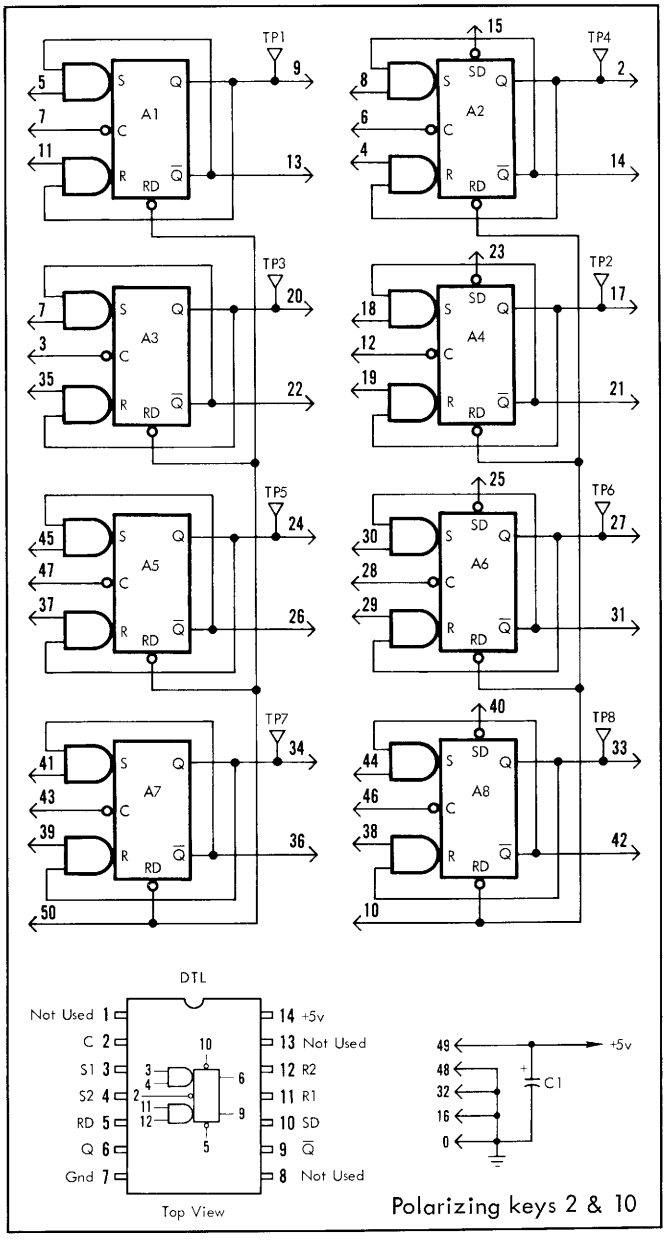
Designator	Description	IC Type	Qty.
A1 thru 8	IC, flip-flop, single	945	8
C1, 2	Cap. mylar, .01μf		2

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			9-1/3
Input loading J and K C and SD Common RD	unit loads	see logic diagram			 2/3 2 8
Propagation delay, at 25°C; loads of 12.8 ma/30 pf	ns			51	81
+5 volt supply (Vcc)	ma			75	83*
Dissipation, per module	mw			375	456*

* at +5.5v

LOGIC DIAGRAM



FJ11
4-BIT BINARY BIDIRECTIONAL COUNTER/REGISTER (DTL)

The FJ11 contains four JK flip-flops and gating to permit operation as a 4-bit synchronous binary up-counter, a 4-bit synchronous binary down-counter, a 4-bit right-shift register, or a 4-bit left-shift register.

Choice of operating mode is made by interconnecting appropriate pins on the module, by making appropriate control lines True or False, and by using the appropriate inputs and outputs, as described below. Data may be preset in any mode, and a Common Reset (clear) line is provided.

The module also contains an independent inverter and an independent NAND available for other use.

Clock, Common Reset, Forward, and Reverse control lines are common to all flip-flops. Set Direct inputs are preceded by gates which provide two separate control (strobe) lines and individual data inputs.

The FJ11 uses DTL circuits. Refer to FJ61 for TTL version.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads				
Q (except Q4)		38, 24, 21			8-1/3
Q4		47			9-1/3
$\overline{Q}$		43, 34, 6, 1			9-1/3
$(\overline{C + B})$		28, 26, 37, 25			6
(C + B)		46, 50, 18, 20			7-1/3
Independent Gates		9, 11			8
Input loading	unit loads				
Forward, Reverse		29, 31			4
Common Reset, Clock		10, 14			1
(C + B) In		19			1
Set-common		5, 40			2
Down-gate		33, 35, 39, 41			1
Gate-common		30, 22, 27, 23			2
Reset (clocked)		45, 36, 7, 3			2/3
Set (direct)		44, 42, 4, 2			1
Independent gates		8, 15, 13			1
Propagation delays (per count or shift) At 25°C, with loads of 12.8 ma/30 pf	ns			60	110
+5 volt supply (Vcc)	ma			73.6	91.8*
Dissipation, per module	mw			368	505*

* at +5.5v

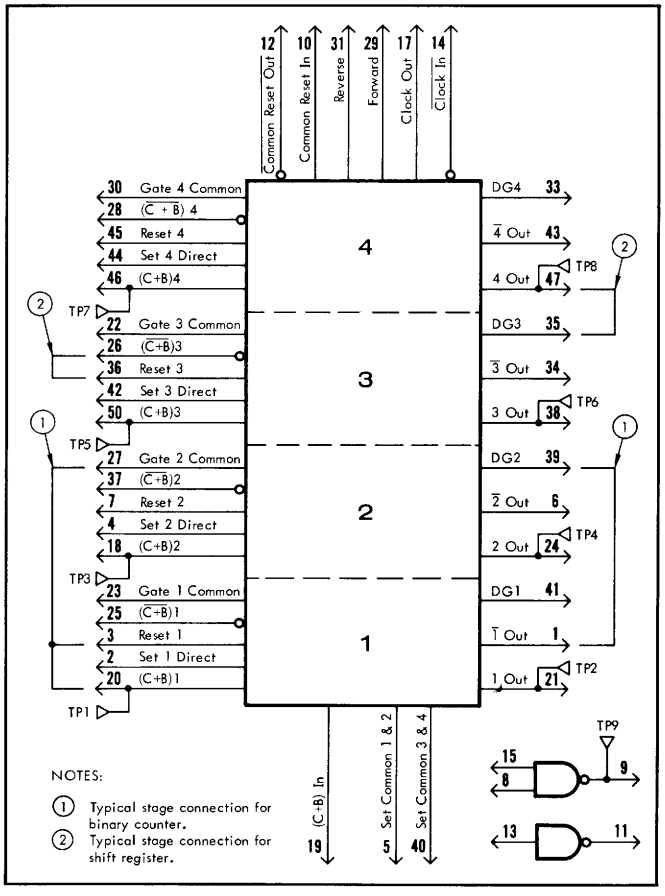
Up-counter

To operate the counter in the up-count (forward) mode: hold the Forward line high (True) and hold the Reverse line low (False); connect each Carry-or-Borrow (C+B) output to the Gate Common input of the suceeding stage, as well as to the clocked Reset input of its own stage. Then clear the counter with Common Reset, and Direct Set data if desired. Raise the (C+B) IN input (Pin 19) and Gate-1-Common (pin 23) high (True), and proceed to increment the counter with a clock.

Down-counter

Connect as for up-counter, except hold Reverse line high (True) and Forward line low (False). Also connect the $\overline{Q}$ output of each stage to the Down-Gate input of the succeeding stage. Raise the Down-Gate-1 (pin 41) and Gate-1-Common (pin 23) high (True) and decrement with a clock.

LOGIC DIAGRAM



Right-shift-register

To operate the module in the right-shift-register (forward) mode: hold the Forward line high (True) and hold the Reverse line low (False); connect each $\overline{(C+B)}$ output to the clocked Reset input of the same stage. Hold the Gate-1-Common (pin 23) high and use (C+B) IN (pin 19) as the shift register data input. Clear the register with Common Reset, if desired, and then preset (Direct Set) data if desired. Shift data into the register through (C+B) IN (pin 19) with a clock for each bit.

Left-shift-register

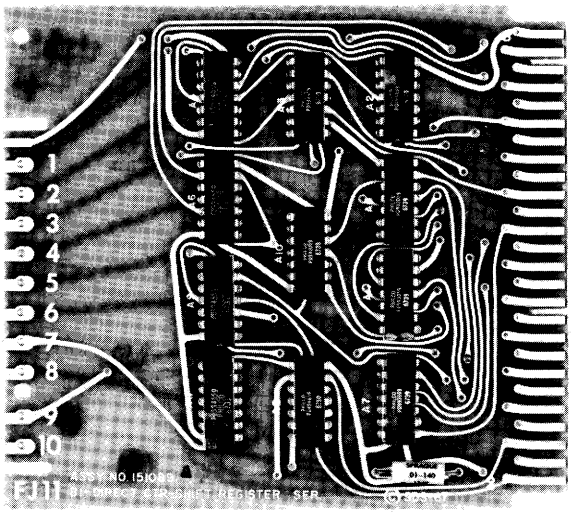
To operate the module in the left-shift-register (reverse) mode: hold the Reverse line high (True) and hold the Forward line low (False); connect each Q output to the Down Gate input of the preceding stage. Hold the Gate-4-Common (pin 30) high and use the Down-Gate-4 input (pin 33) as the shift register data input. Clear the register with Common Reset, if desired, and then preset (Direct Set) data if desired. Shift data into the register through Down-Gate-4 (pin 33) with a clock for each bit.

Variations

The module can be wired to count in any desired pattern other than straight binary, or shift in any 4-bit sequence. External gating can also be interposed between stages when needed. Modules can be cascaded to form any desired length counter or register. Since counting is synchronous, delay remains the same and is independent of counter length.

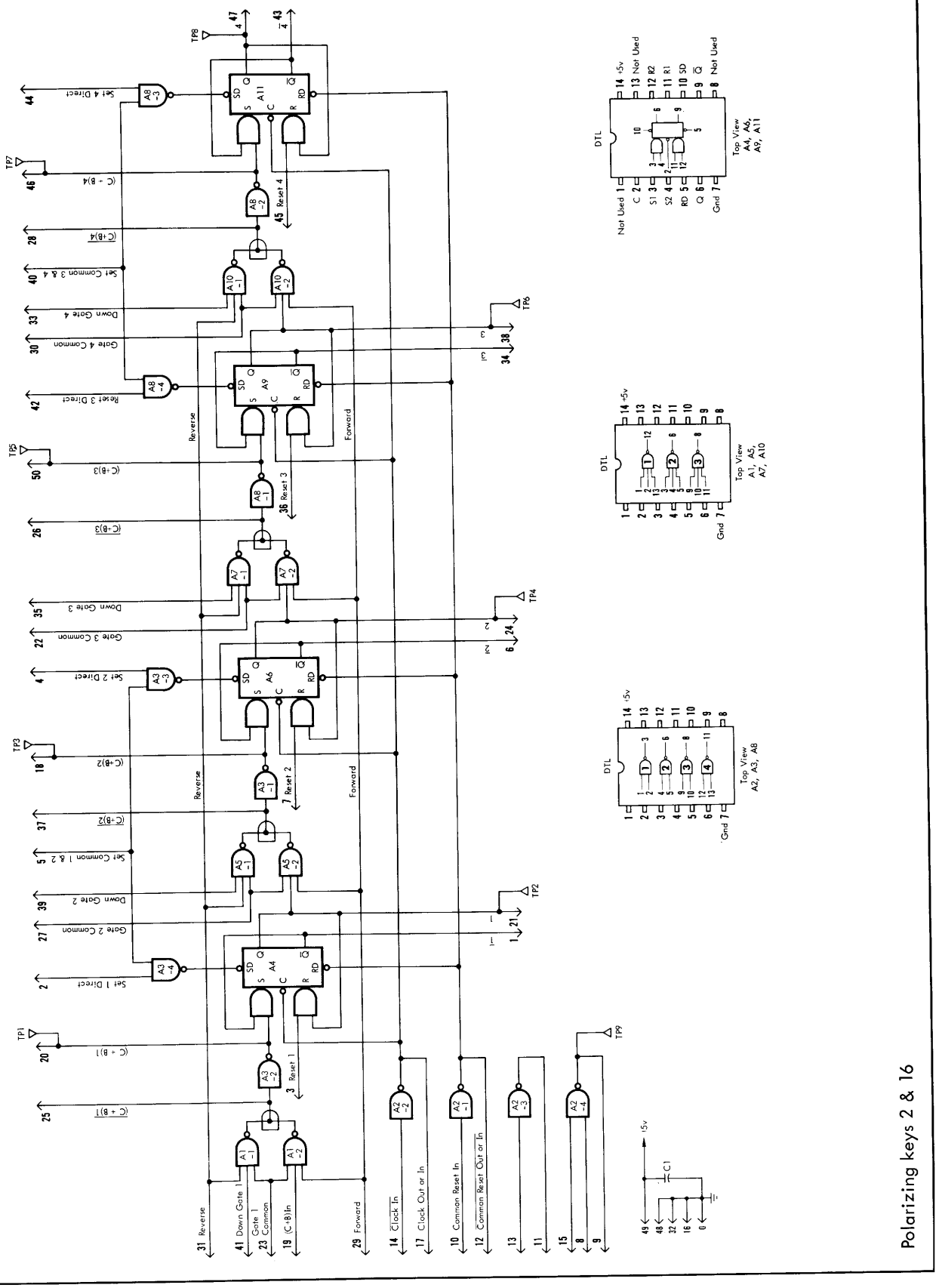
PARTS LIST

Designator	Description	Type	Qty.
A1, 5, 7, 10	IC gate, dual 4-in	930	4
A4, 6, 9, 11	IC flip-flop, single	945	4
A2, 3, 8	IC gate, quad 2-in	946	3
C1	Cap., mylar, .01μf		1



(Refer to page 44 for circuit schematic diagram)

SCHEMATIC DIAGRAM, FJ11



The FJ12 module contains five gated, clocked RS flip-flops. Each S and R input is preceded by a 2-input AND gate. Logic levels appearing at these gates enter the flip-flop only in conjunction with a clock signal.

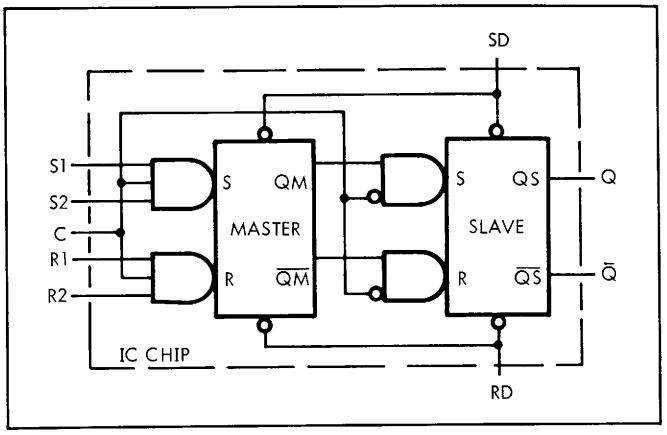
Each RS flip-flop contains a master and a slave flip-flop placed on the same IC chip, functionally related as shown in the diagram at right. The clock signal, when high, moves S or R input data into the master flip-flop. When it goes low it causes data to transfer to slave. The clock input is shown with an inversion symbol to indicate that data appears at the outputs when clock goes low.

The direct inputs (SD and RD) override the clocked S and R inputs. A low level (0v) activates SD or RD.

Truth table is given at the beginning of this section, under the heading "Logic Symbols". Note that the RS flip-flop has an ambiguous state. When S and R are both high simultaneously, it is not possible to predict the state that results after the clock. A JK hookup avoids this ambiguity. This consists of connecting Q output to R1 or R2 input, and $\overline{Q}$ output to S1 or S2 input. Refer to FJ10 for a JK module.

The clock should have a minimum True (high) time of 100 nsec and a minimum False (low) time of 100 nsec. Logic levels at the S and R inputs must be stable for the entire clock high time.

The FJ12 uses DTL circuits. Refer to FJ62 for TTL version.

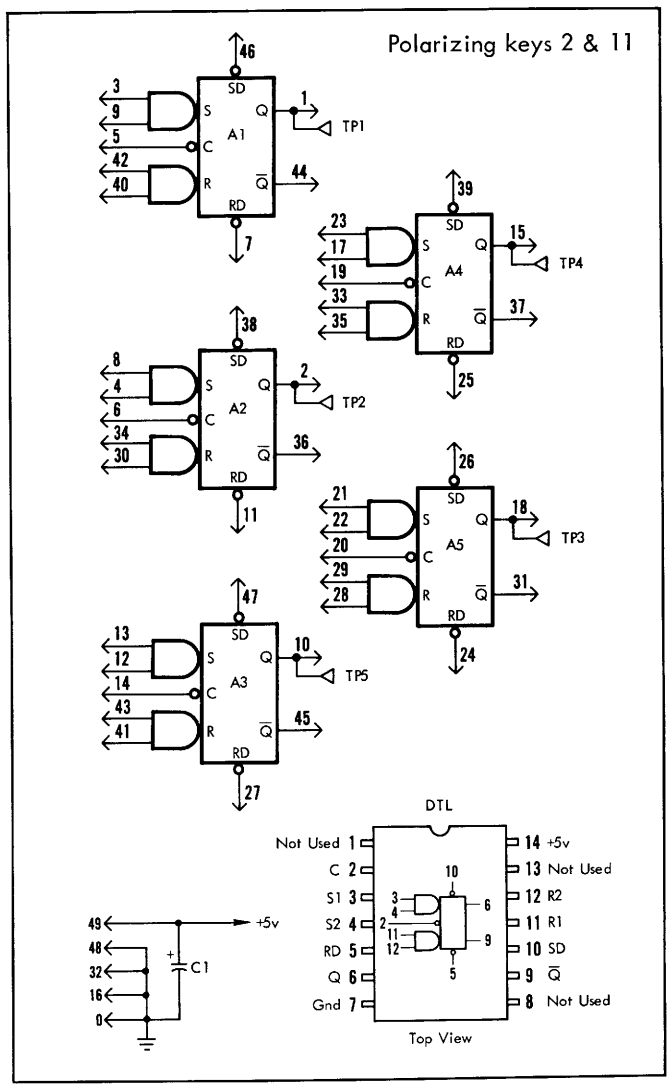


SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			10
Input loading S1, S2, R1, R2 C, SD, RD	unit loads	see logic diagram			 2/3 2
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			51	81
+5 volt supply (Vcc)	ma			47	52*
Dissipation, per module	mw			235	286*

* at +5.5v

LOGIC DIAGRAM



PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 5	IC, flip-flop, single	945	5
C1	Cap. mylar, .01μf		1

FJ13
4-BIT BUFFER STORAGE REGISTERS (DTL)

The FJ13 module contains four 4-bit buffer storage registers. It is constructed entirely of 2-input NANDs, arranged as buffered latches with strobed gates at inputs and outputs. Each 4-bit section is independent of the others, and has its own common reset line, set strobe (load strobe), and readout strobe. Only the complement of the input data is available at the outputs.

The set strobe and readout strobe are normally low (logic 0) and must be raised high (logic 1) to load or read the register. The reset strobe is normally high and must be made low to clear the register.

FJ13 uses DTL circuits. Refer to FJ63 for TTL version.

SPECIFICATIONS

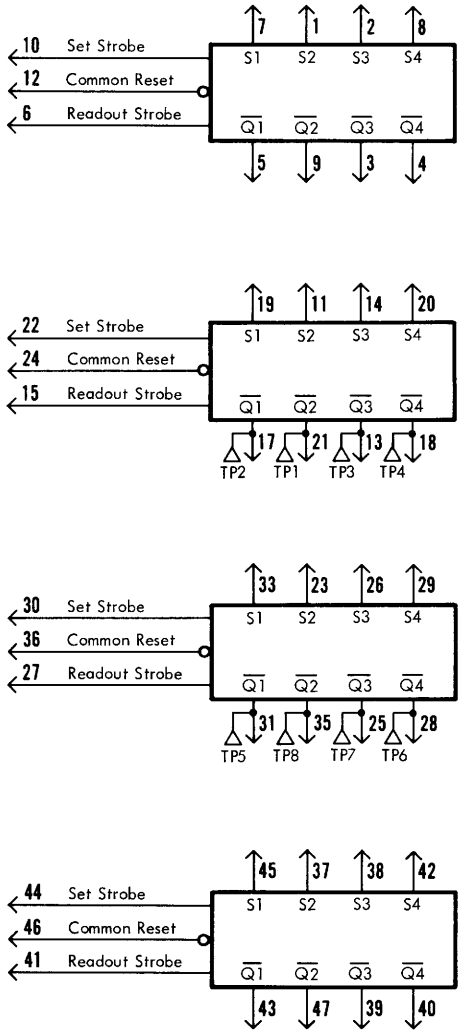
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			8
Input loading S1, S2, S3, S4 Strobe or reset	unit loads	see logic diagram			 1 4
Timing, at 25°C with loads of 12.8ma/30pf	Data inputs must be stable for 88 ns min., beginning at set strobe leading edge. Set strobe must be min. 88 ns in duration. Data is available 31 ns (typ) after readout strobe leading edge. Reset must be low for 88 ns.				
+5 volt supply (Vcc)	ma			115	161.3*
Dissipation, per module	mw			575	887*

* at +5.5v

PARTS LIST

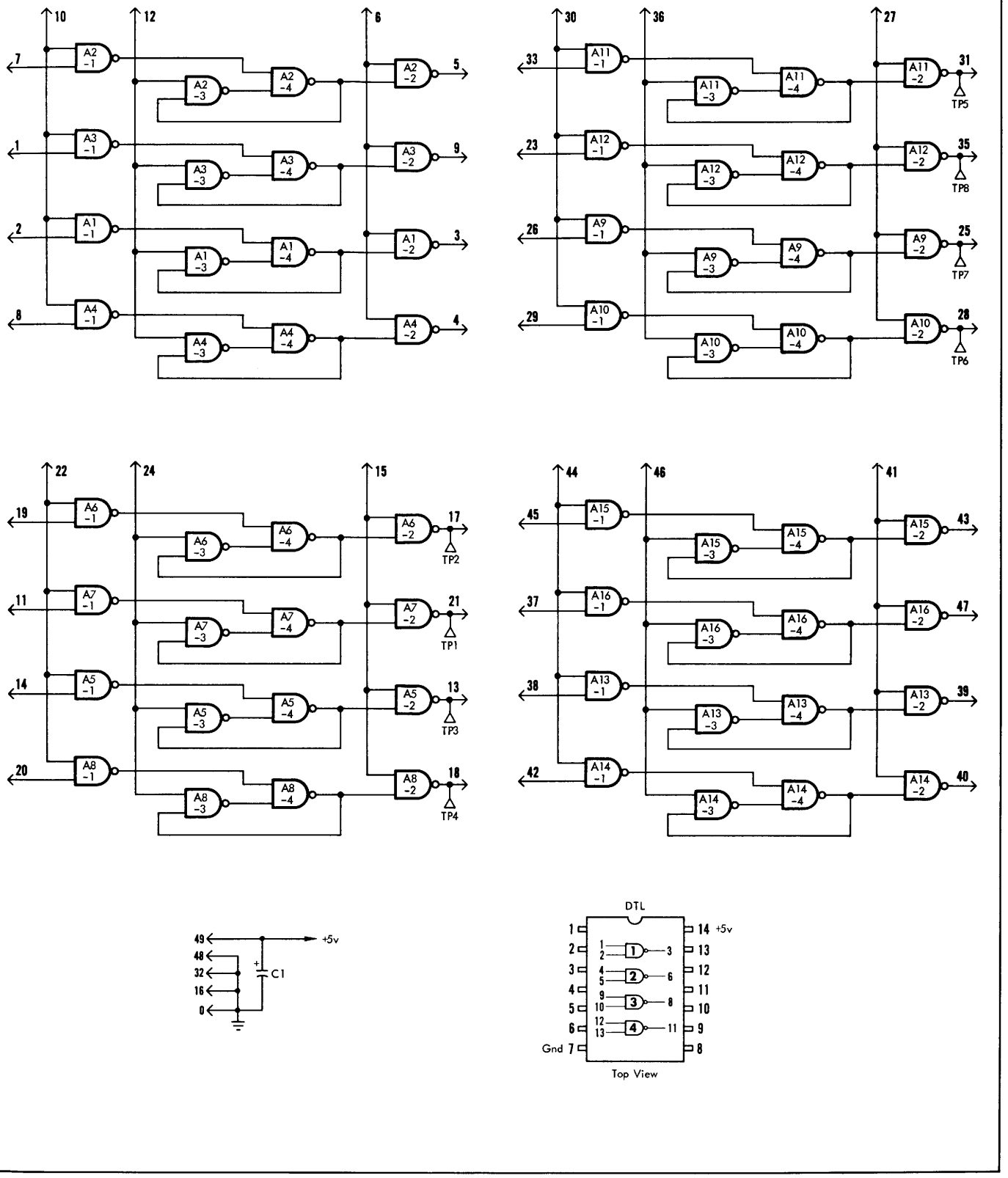
Designator	Description	Type	Qty,
A1 thru A16	IC gate, quad 2-in	946	16
C1	Cap., mylar, .01μf		1

LOGIC DIAGRAM



Polarizing keys 2 & 13

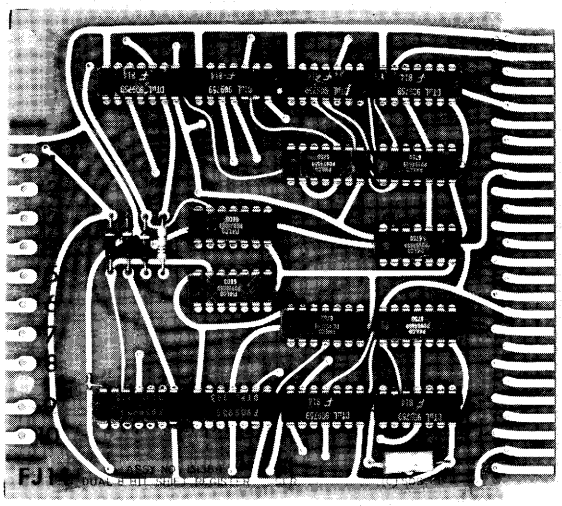
SCHEMATIC DIAGRAM, FJ13



FJ14
8-BIT SHIFT REGISTERS (DTL)

The FJ14 contains two independent 8-bit shift registers which can be used for serial-input to parallel-output, parallel input to serial-output, or simple parallel-parallel storage. Common gated clock and reset inputs are provided. Strobed direct-set inputs, used for presetting, are also provided. A test point is provided at module front edge for each Q output of one register, and for Q7 and Q8 outputs of the other.

This module uses DTL circuits. Refer to FJ64 for TTL version



SPECIFICATIONS

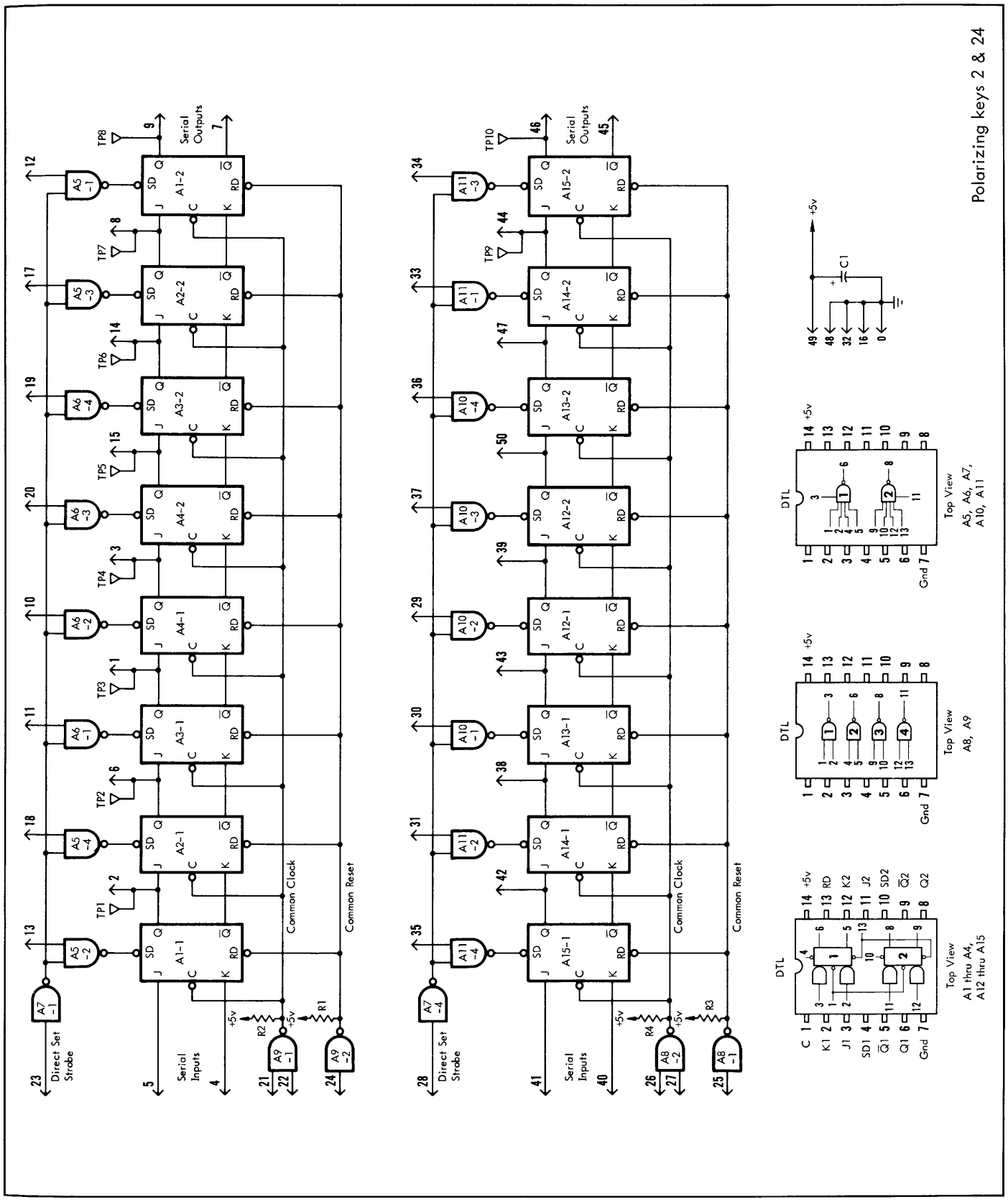
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	9, 7, 46, 45 all others			10 9
Input loading	unit loads	5, 4, 41, 40 all others			2/3 1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			87	137
+5 volt supply (Vcc)	ma			202	233*
Dissipation, per module	watts			1.0	1.28*

* at +5.5v

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 4, A12 thru 15	IC, flip-flop, dual	9099	8
A5, 6, 7, 10, 11	IC, gate, quad 2-in	946	5
A8, 9	IC, power gate	944	2
R1 thru 4	Res., 1.1KΩ, 1/4w		4
C1	Cap., mylar, .01μf		1

LOGIC DIAGRAM, FJ14



FJ16
BCD UP-COUNTER/DECODER (DTL)

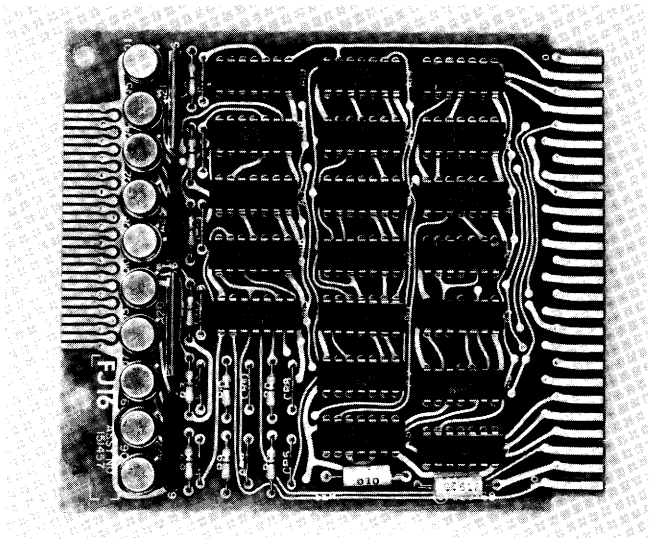
The FJ16 contains a 4-bit BCD ripple-through up-counter and a BCD to 10-line decoder. The decoder has both logic-level outputs and high current outputs which can be used to directly drive lamps or relays. The counter has strobed individual direct-set inputs for presetting, as well as a gated common reset line.

Certain terminals must be externally jumpered on the back plane, as shown in Table 1 in the logic diagram.

All three functions -- counting, 10-line decoding, and display driving -- are mounted on one module, reducing to one slot the mounting space required for one displayed decade.

The decoder-driver section is identical to the BJ10 module. The FJ16 uses the same general purpose etch pattern as the BJ10, BJ11, and FJ17 modules, filled with ICs as shown in the photograph at right.

The FJ16 uses DTL circuits. For a TTL version of this logic structure refer to FJ66.



PARTS LIST

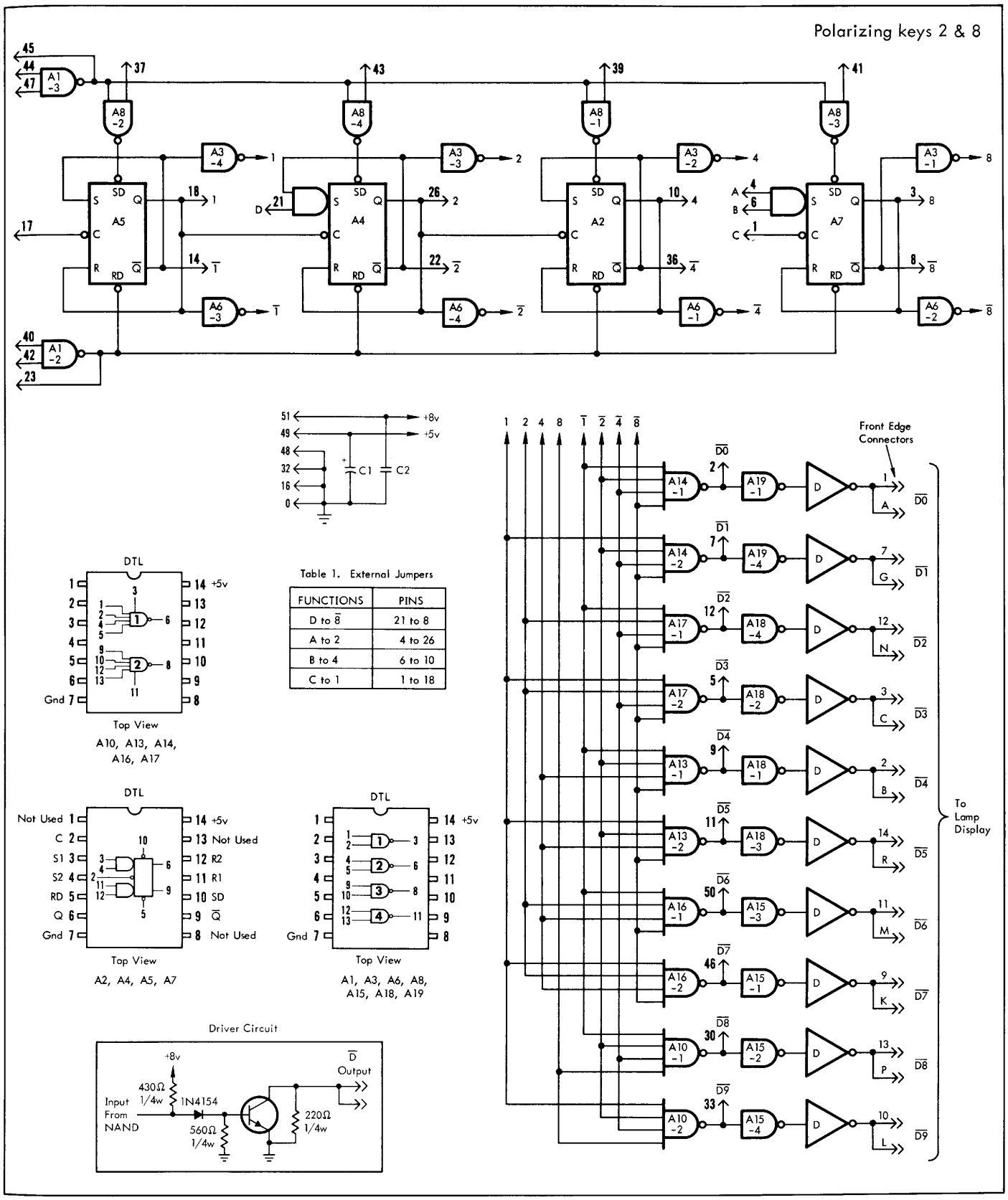
Designator	Description	IC Type	Qty.
A2, 4, 5, 7	IC flip-flop, single	945	4
A1, 3, 6, 8, 15, 18, 19	IC gate, quad 2-in	946	7
A10, 13, 14, 16, 17	IC gate, dual 4-in	930	5
A20, 21	Res. network, 220Ω, 1/4w		2
A22, 23	Res. network, 560Ω, 1/4w		2
R1 thru 10	Res., 430Ω, 1/4w		10
CR1 thru 10	Diode	1N4154	10
Q1 thru 10	Transistor	2N3722	10
C1, 2	Cap. mylar, .01μf		2

SPECIFICATIONS

Characteristics	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out into, DTL (at NAND outputs)	unit loads	14, 22, 36, 3 all others			8 7
Current per lamp driver (at 28vdc max.)	ma	front edge			200
Keep-alive resistor (designed for use with 5v bulb; remove if v exceeds 8v)	ohms watts			220 1/4	
Input loading	unit loads	45, 23 all others			6 1
Propagation delay, at 25°C, with loads of 11.2 ma/30 pf	ns			260	420
+5 volt supply (Vcc)	ma			98.8	127*
+8 volt supply	ma			198	216
Dissipation, per module	watts			2.08	2.60*

* at +5.5v

LOGIC DIAGRAM, FJ16



FJ17
BINARY UP-COUNTER WITH 16-LINE DECODER (DTL)

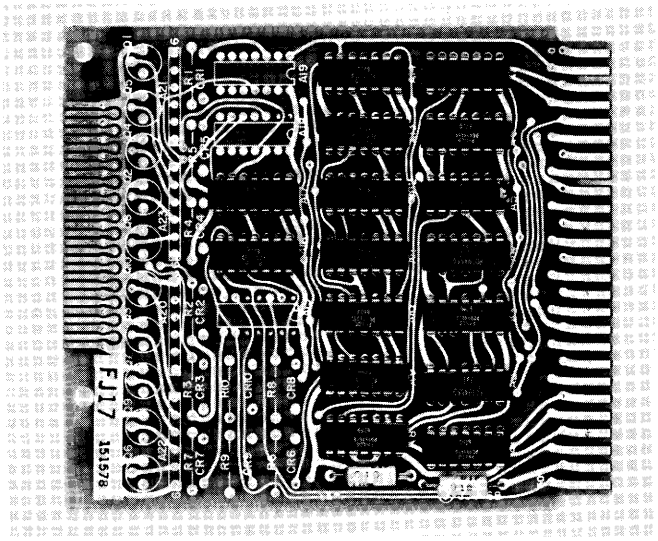
The FJ17 contains a 4-bit binary ripple-through up-counter and a binary to 16-line decoder. The counter has strobed individual direct-set inputs for presetting, as well as a gated common reset line.

Certain terminals must be externally jumpered on the back-plane, as shown in Table 1 in the logic diagram.

Two functions -- counting and decoding -- are mounted on one module, providing extremely high packing density.

The decoder section is identical to the BJ11 module. The FJ17 uses the same general purpose etch pattern as the BJ10, BJ11, and FJ16 modules, filled with ICs as shown in the photograph at right.

The FJ17 uses DTL circuits. For a TTL version of this logic structure refer to FJ67.



PARTS LIST

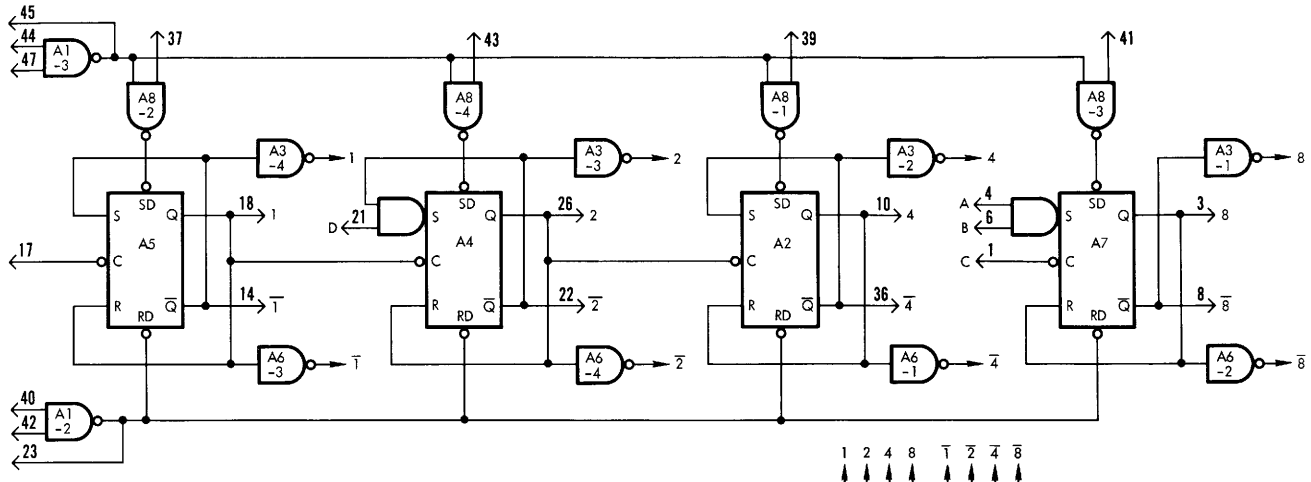
Designator	Description	Type	Qty.
A2, 4, 5, 7	IC flip-flop, single	945	4
A1, 3, 6, 8	IC gate, quad, 2-in	946	4
A9, 10, 11, 12, 13, 14, 16, 17	IC gate, dual 4-in	930	8
C1, 2	Cap., mylar, .01μf		2

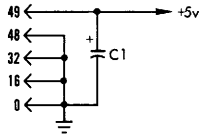
SPECIFICATIONS

Characteristics	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	18, 26, 10, 8 all others			7 8
Input loading	unit loads	45, 23 all others			6 1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			260	420
+5 volt supply (Vcc)	ma			91.6	117*
Dissipation, per module	mw			458	643*

* at +5.5v

LOGIC DIAGRAM, FJ17





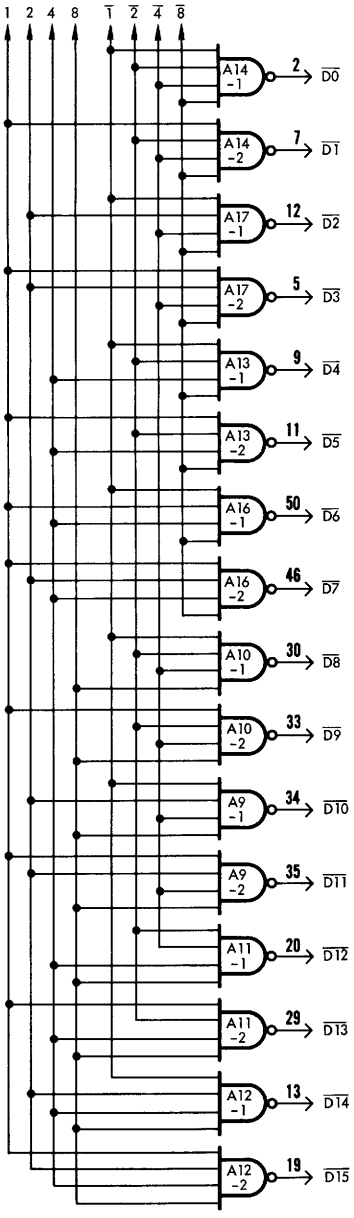
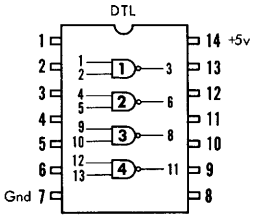
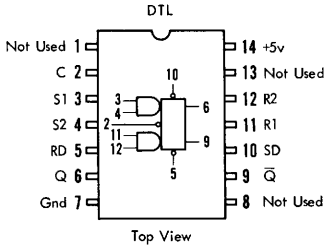


Table 1. External Jumpers

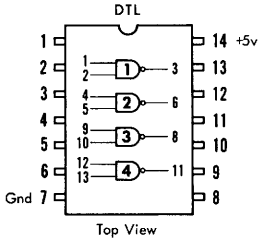
FUNCTIONS	PINS
A to $\overline{8}$	4 to 8
C to 4	1 to 10



A1, A3, A6, A8



A2, A4, A5, A7



A9 thru A14,
A16, A17

Polarizing keys 2 & 8

FJ18
BCD BIDIRECTIONAL COUNTER, 3 DECADES (DTL)

This module contains three identical decades of clocked BCD counting on one module. It functions as either up-counter or down-counter, depending on whether the control signals at pins 9, 25, and 41 are high (up) or low (down).

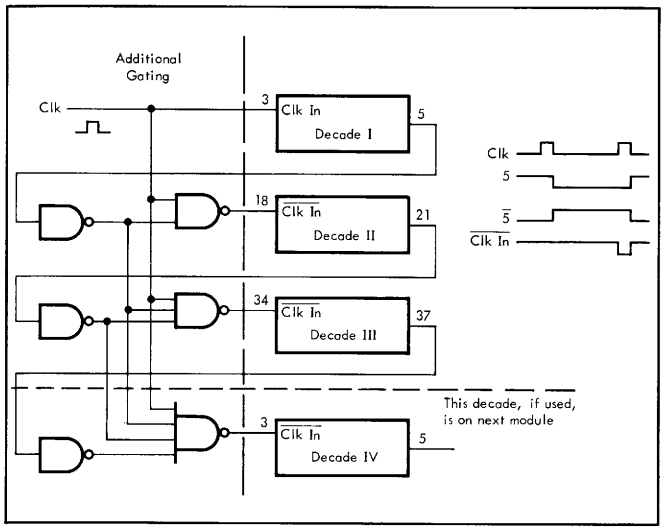
Common clock, common reset, and commonly strobed preset inputs are provided for each decade. The clock and reset inputs are provided with inverters so that either logic phase (signal or complement) can be used. In addition, each inverter can be used to gate the other input, using the wired-logic principle. For example, if the input at pin 2 is held high (logic 1), then the input at pin 3 cannot rise because the inverter output holds it low.

Each decade has a clock output (pins 5, 21, 37) which is used to provide clock input to the next decade, when two decades are serially chained together. If counting direction will remain stable, clock output can connect directly to next input. If up/down changeover during operation is anticipated, use additional gating as shown at right.

Front-edge test points are provided at the Q outputs of ten of the twelve counter flip-flops.

This module uses DTL circuits. A TTL version of a similar logic structure is the FJ68.

The FJ18 will conveniently interface with the BJ12.



Gating Required For Dynamic Up/Down Transition

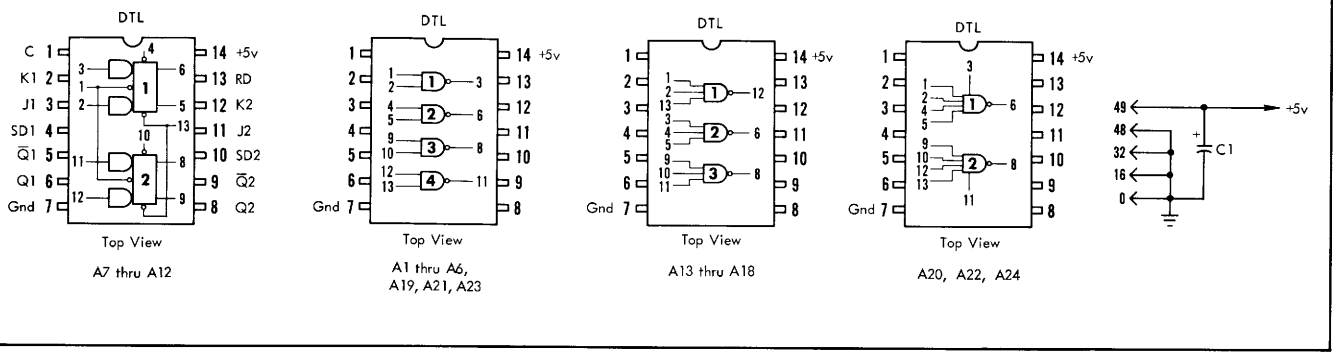
PARTS LIST

Designator	Description	Type	Qty.
A1 thru 6, A19, 21, 23	IC gate, quad 2-in	946	9
A13 thru 18	IC gate, triple 3-in	962	6
A20, 22, 24	IC gate, dual 4-in	930	3
A7 thru 12	IC flip-flop, dual	9099	6
C1	Cap., mylar, .01μf		1
CR1, 2, 3	Diode	1N4154	3

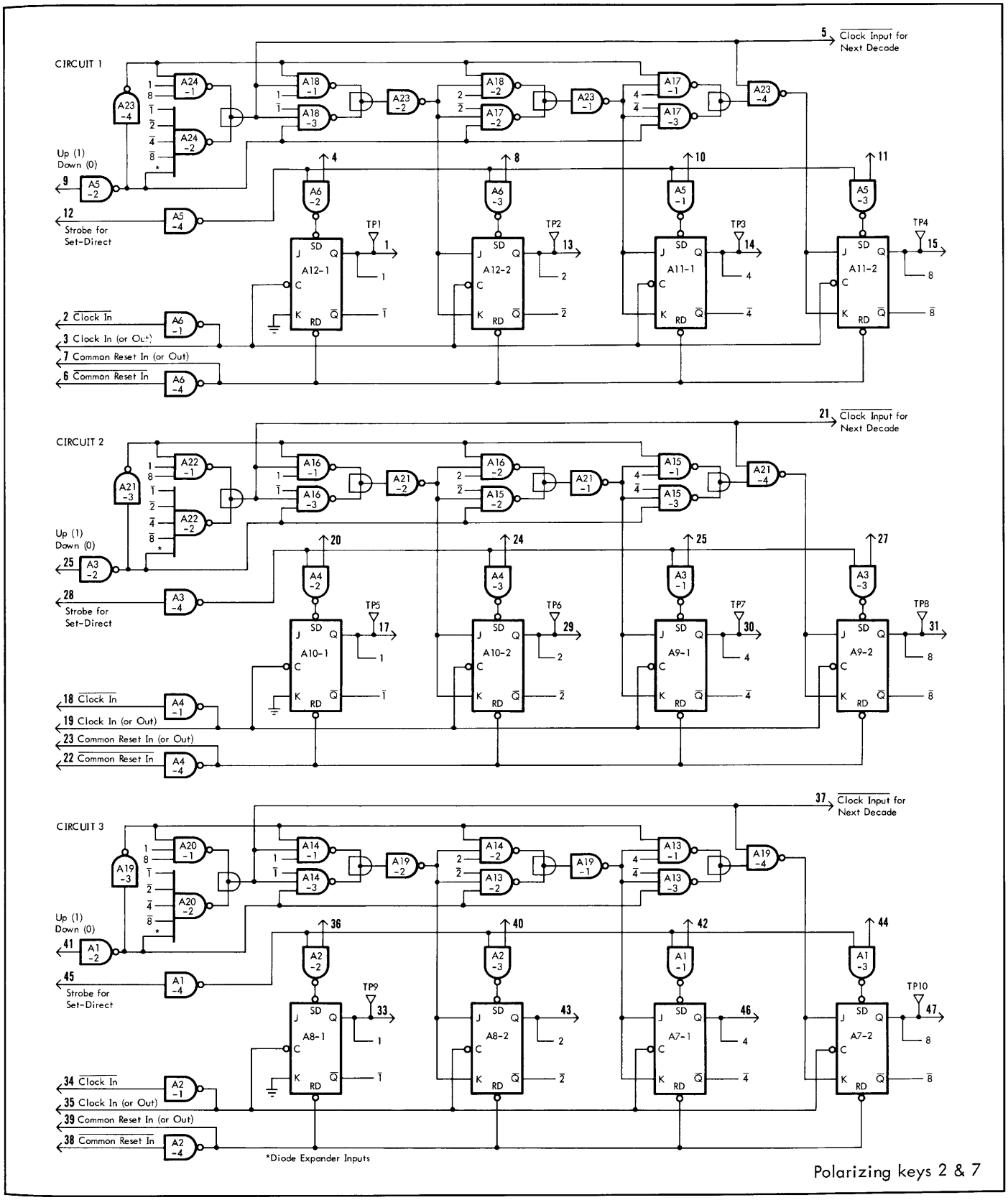
SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	5 1, 17, 33 all others			4 8 9
Input loading	unit loads	3, 19, 35, 7, 23, 39 all others			9 1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			140	230
+5 volt supply (Vcc)	ma			220.8	275.3*
Dissipation, per module	watts			1.1	1.5*

* at +5.5v



LOGIC DIAGRAM, FJ18



Polarizing keys 2 & 7

FJ19, FJ20, FJ21
STORAGE REGISTERS, 8-BIT, 10-BIT, 12-BIT (DTL)

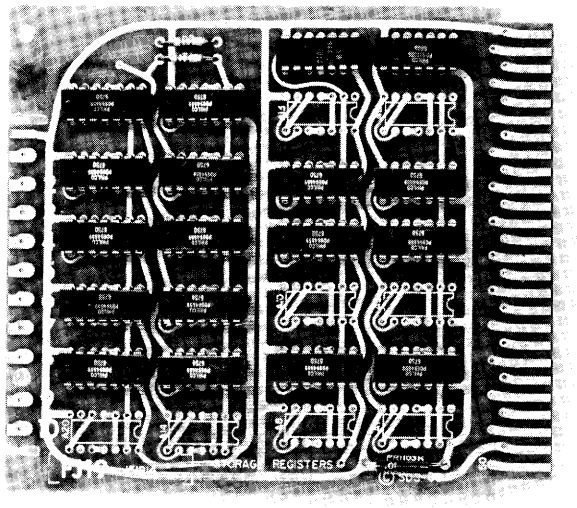
The FJ19, FJ20, and FJ21 are high-density buffered-latch storage register modules. Each module contains two registers. The two FJ19 registers have 8 bits each; FJ20 registers have 10 bits each; and FJ21 registers have 12 bits each.

One logic diagram is shown to describe all three registers. All three module types use the same basic etched circuit board. Each is filled with only the ICs required to perform its function.

Two common control lines are provided on each module, one for each register. When the control line inputs are all high, the control line goes high. Each control line strobes into all flip-flops under its control the signal that is present on the input line. If the input signal is high, Q output goes high.

Test points are provided on the outputs of one of the two registers on each module, as shown in the logic diagram.

These register modules are offered only in a DTL version.



SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			7
Input loading Signal inputs Strobe inputs	unit loads	see logic diagram			 2 1
Propagation delay per stage, at 25°C, with loads of 11.2 ma/30 pf	ns			180	300
+5 volt supply (Vcc) FJ19 FJ20 FJ21	ma			 128 155.8 185.8	 176.7* 217* 258*
Dissipation, per module FJ19 FJ20 FJ21	mw			 646 779 929	 974* 1,190* 1,420*

* at +5.5v

PARTS LIST, FJ19

Designator	Description	Type	Qty.
A26	IC, power gate	944	1
A2, 4, 5, 9, 11, 12, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25	IC gate, quad 2-in	946	16
A7	IC gate, dual 4-in	930	1
C1	Cap., mylar, .01μf		1
R1, 2	Res., 1.1KΩ, 1/4w		2

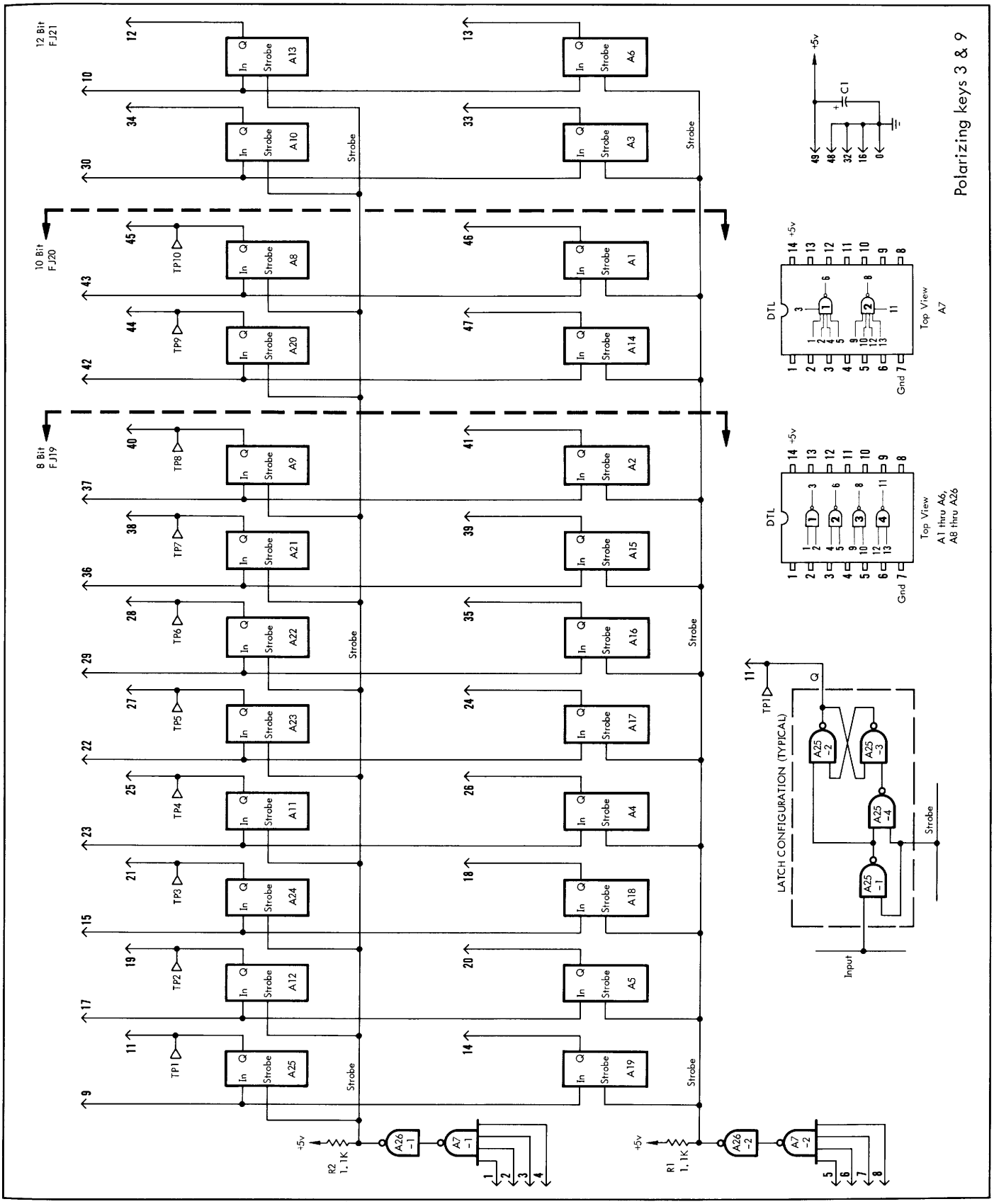
PARTS LIST, FJ20

Designator	Description	Type	Qty.
A26	IC power gate	944	1
A1, 2, 4, 5, 8, 9, 11, 12, 14 thru 25	IC gate, quad 2-in	946	20
A7	IC gate, dual 4-in	930	1
C1	Cap., mylar, .01μf		1
R1, 2	Res., 1.1KΩ, 1/4w		2

PARTS LIST, FJ21

Designator	Description	Type	Qty.
A26	IC power gate	944	1
A1 thru 6, A8 thru 26	IC gate, quad 2-in	946	24
A7	IC gate, dual 4-in	930	1
C1	Cap., mylar, .01μf		1
R1, 2	Res., 1.1KΩ, 1/4w		2

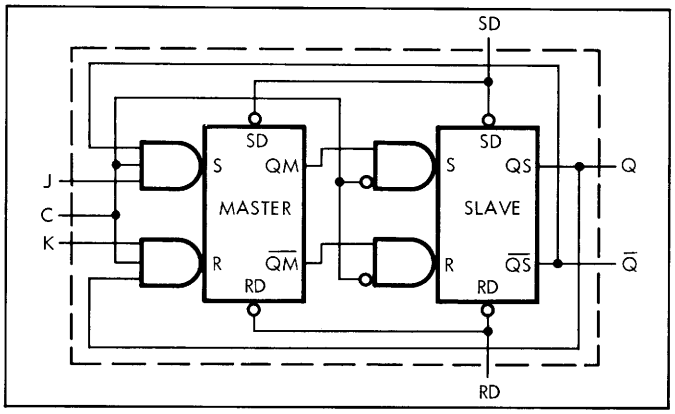
LOGIC DIAGRAM, FJ19/FJ20/FJ21



FJ60
JK FLIP-FLOPS (TTL)

The FJ60 module contains eight JK flip-flops, with two common Reset Direct (clear) lines. One group of four also has individual Set Direct inputs.

Each JK flip-flop is a clocked storage element consisting of a master and a slave flip-flop placed on the same IC chip, functionally related as shown in the diagram below. The master-slave principle has the advantage that the circuit is not sensitive to rise or fall times of clock signals, or to clock pulsewidth, providing that the pulse width exceeds the minimum required for internal propagation delays. The clock signal, when low, moves J or K input data into the master flip-flop; when it goes high it causes data to transfer from master to slave.



The FJ60 Set Direct (SD) and Reset Direct (RD) inputs override the clocked (J and K) inputs. A low level (0v) is used to activate SD or RD.

Truth table is given at the beginning of this section, under the heading "Logic Symbols".

The FJ60 uses TTL circuits. Refer to FJ10 for DTL version.

PARTS LIST

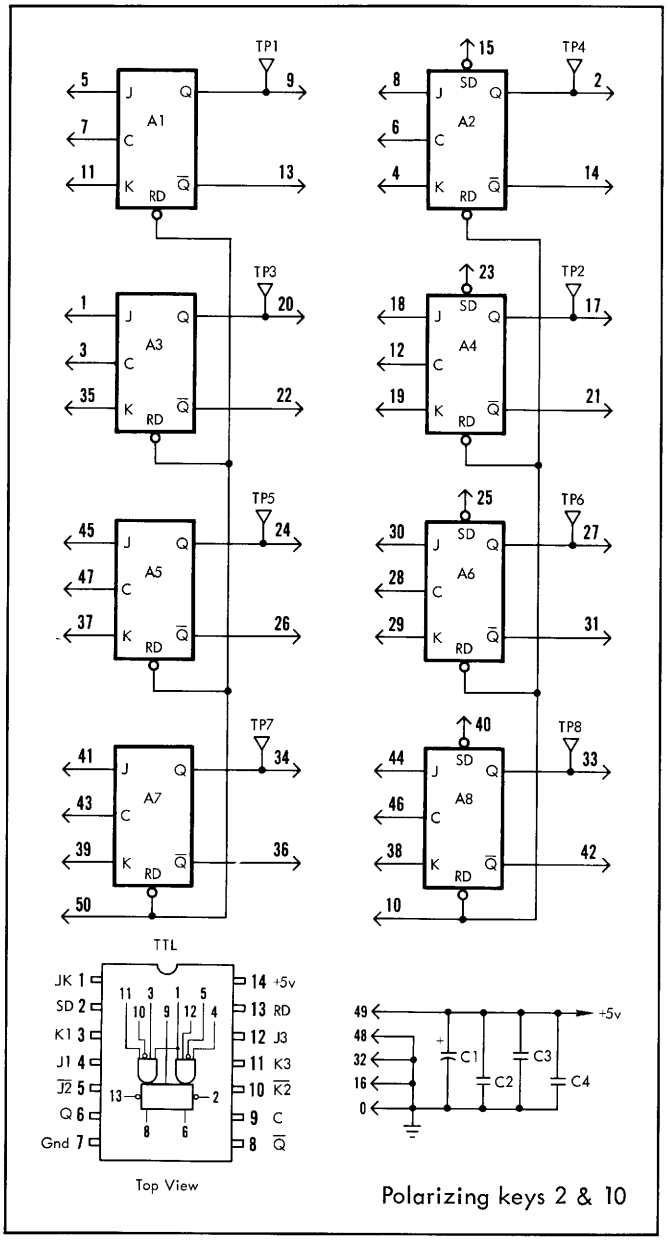
Designator	Description	IC Type	Qty.
A1 thru 8	IC, flip-flop, single	9001	8
C1	Cap., tantalum 1μf		1
C2, 3, 4	Cap., mylar .01μf		3

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads				8
Input loading	unit loads	15, 23, 25, 40 10, 50 all others			2.7 10.8 1
Propagation delay, at 25°C, with loads of 15pf	ns			17	32
+5 volt supply (Vcc)	ma			120	220*
Dissipation, per module	mw			600	1,210*

* at +5.5v and 20 MHz

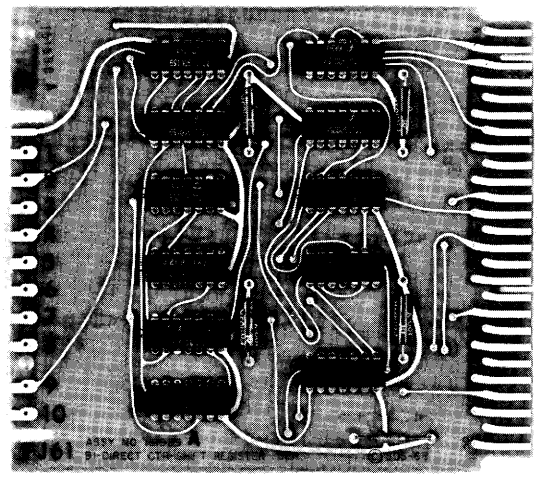
LOGIC DIAGRAM



(TTL) 4-BIT BINARY BIDIRECTIONAL COUNTER/REGISTER

The FJ61 contains four JK flip-flops and gating to permit operation as a 4-bit synchronous binary up-counter, a 4-bit synchronous binary down-counter, a 4-bit right-shift register, or a 4-bit left-shift register.

Choice of operating mode is made by interconnecting appropriate pins on the module, by making appropriate control lines True or False, and by using the appropriate inputs and outputs. Refer to FJ11 description to obtain detailed directions for operating the module in the desired mode.



PARTS LIST

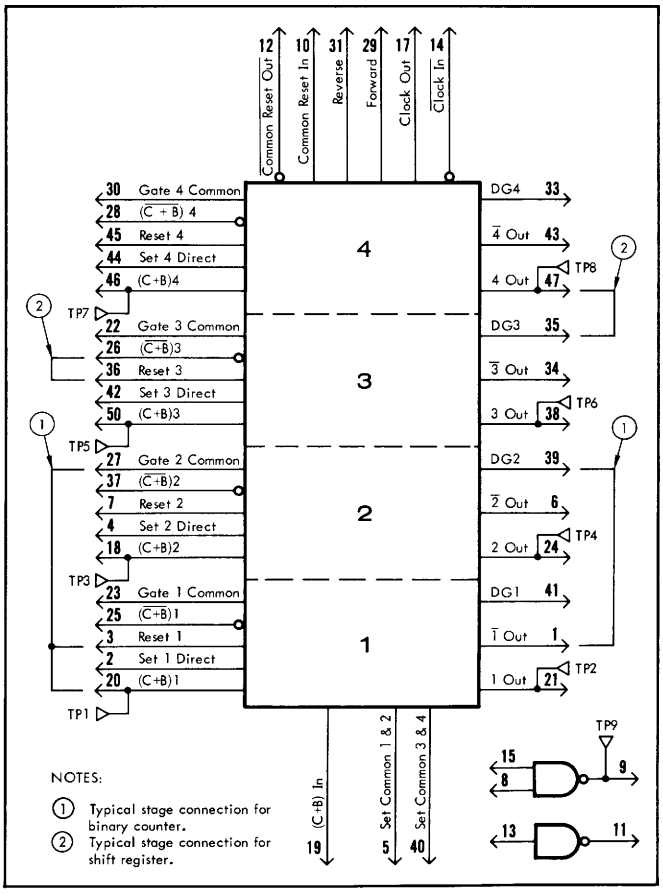
Designator	Description	Type	Qty.
A1, 4, 5, 9	IC gate, quad 2-in	9002	4
A6, 7, 10, 11	IC flip-flop, single	9001	4
A8, 2, 13	IC gate, triple 3-in	9003	3
C2, 3, 4, 5	Cap., mylar, .01μf		4
C1	Cap., tantalum, 1μf		1

SPECIFICATIONS

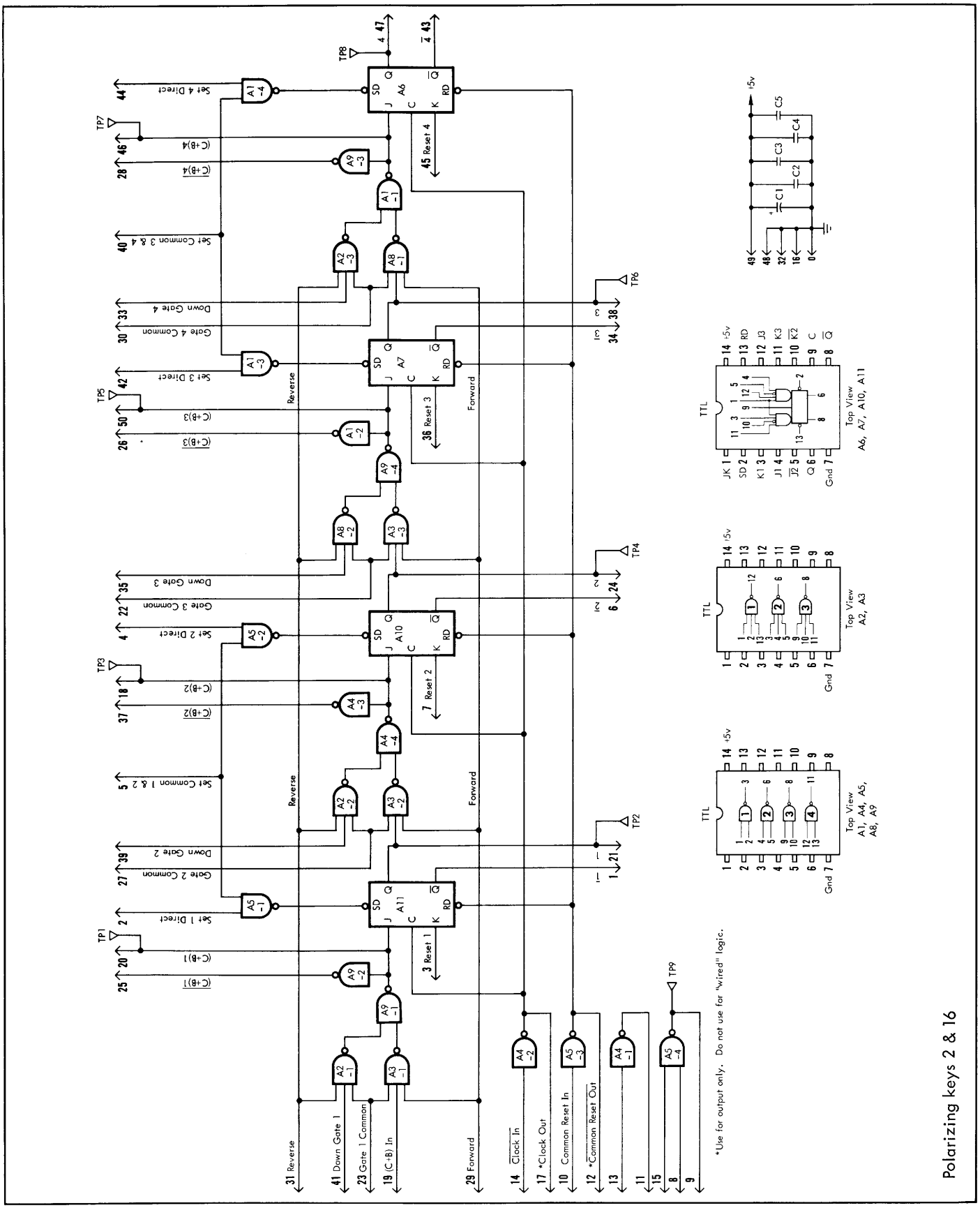
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads				
Q (except Q4)		38, 24, 21			7
Q4		47			8
$\overline{Q}$		43, 34, 6, 1			8
$\overline{(C + B)}$		28, 26, 37, 25			8
(C + B)		46, 50, 18, 20			6
Independent gates		9, 11			8
Input loading	unit loads				
Forward; Reverse		29, 31			4
Common Reset, Clock		10, 14			1
(C + B) In		19			1
Set-common		5, 40			2
Down-gate		33, 35, 39, 41			1
Gate-common		30, 22, 27, 23			2
Reset (clocked)		45, 36, 7, 3			1
Set (direct)		44, 42, 4, 2			1
Independent gates		8, 15, 13			1
Propagation delay, at 25°C, with loads of 15pf	ns			37	60
+5 volt supply (Vcc)	ma			103	374*
Dissipation, per module	mw			517	2,060*

* at +5.5v and 20 MHz

LOGIC DIAGRAM



SCHEMATIC DIAGRAM, FJ61



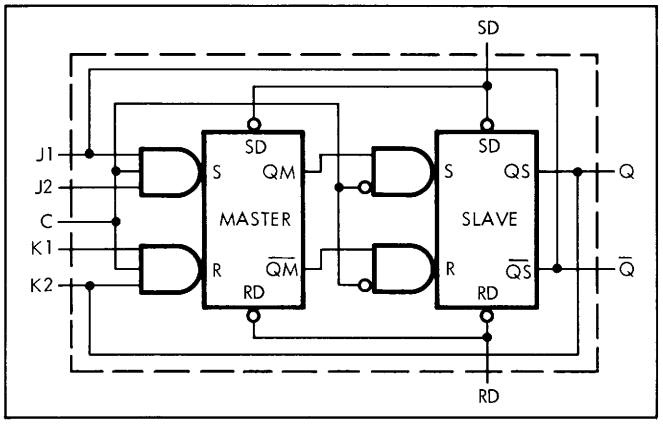
The FJ62 module contains five independent, gated, clocked JK flip-flops. Each J and K input is preceded by a 2-input AND gate. Logic levels appearing at these gates enter the flip-flop only in conjunction with a clock signal.

Each JK flip-flop contains a master and a slave flip-flop placed on the same IC chip, functionally related as shown in the diagram at right. The clock signal, when low, moves J or K input data into the master flip-flop. When it goes high it causes data to transfer to slave.

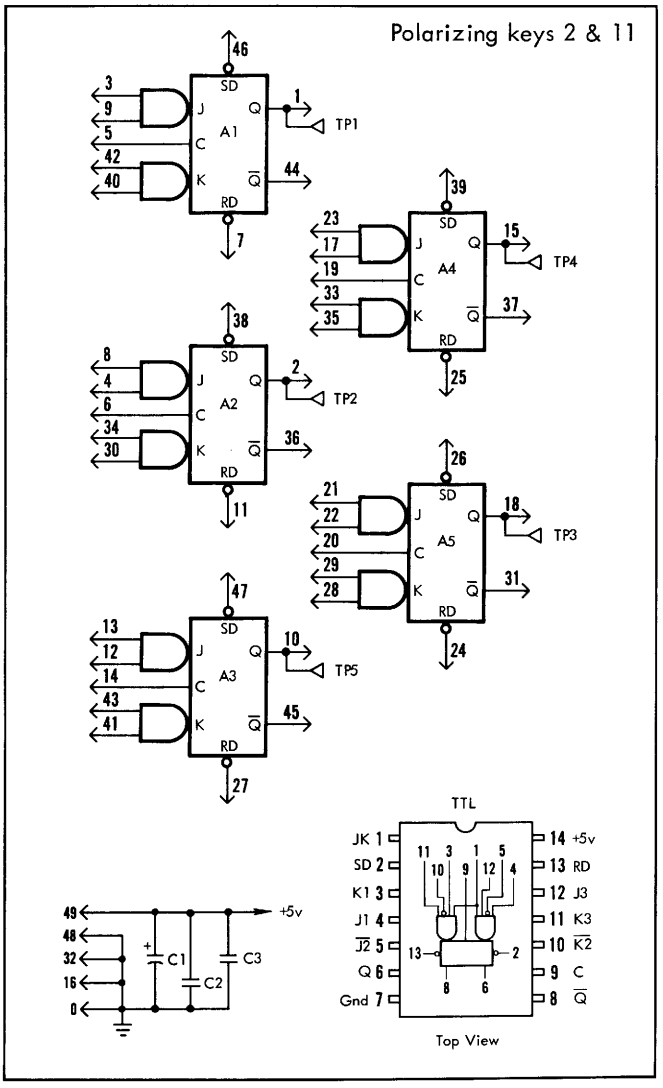
The direct inputs (SD and RD) override the clocked J and K inputs. A low level (0v) activates SD or RD.

Truth table is given at the beginning of this section, under the heading "Logic Symbols". Note that the JK flip-flop does not have an ambiguous state.

This module is pin-for-pin compatible with the FJ12 module. However, this module uses JK flip-flops, while the FJ12 uses RS flip-flops. If a direct substitution of the FJ12 is made for FJ62, external J and K feedback paths may need to be added to the FJ62 wiring to eliminate input ambiguities.



LOGIC DIAGRAM



SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			8
Input loading J, K, C inputs SD, RD inputs	unit loads	see logic diagram			 1 2.7
Propagation delay, at 25°C, with loads of 15pf	ns			17	32
+5 volt supply (Vcc)	ma			75	137.5*
Dissipation, per module	mw			375	756*

* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 5	IC, flip-flop, single	9001	5
C1	Cap. tantalum, 1μf		1
C2, 3	Cap. mylar, .01μf		2

FJ63
4-BIT BUFFER STORAGE REGISTERS (TTL)

The FJ63 module contains four 4-bit buffer storage registers. It is constructed entirely of 2-input NANDs, arranged as buffered latches with strobed gates at inputs and outputs. Each 4-bit section is independent of the others, and has its own common reset line, set strobe (load strobe), and readout strobe. Only the complement of the input data is available at the outputs.

The set strobe and readout strobe are normally low (logic 0) and must be raised high (logic 1) to load or read the register. The reset strobe is normally high and must be made low to clear the register.

The FJ63 uses TTL circuits. Refer to FJ13 for DTL version.

SPECIFICATIONS

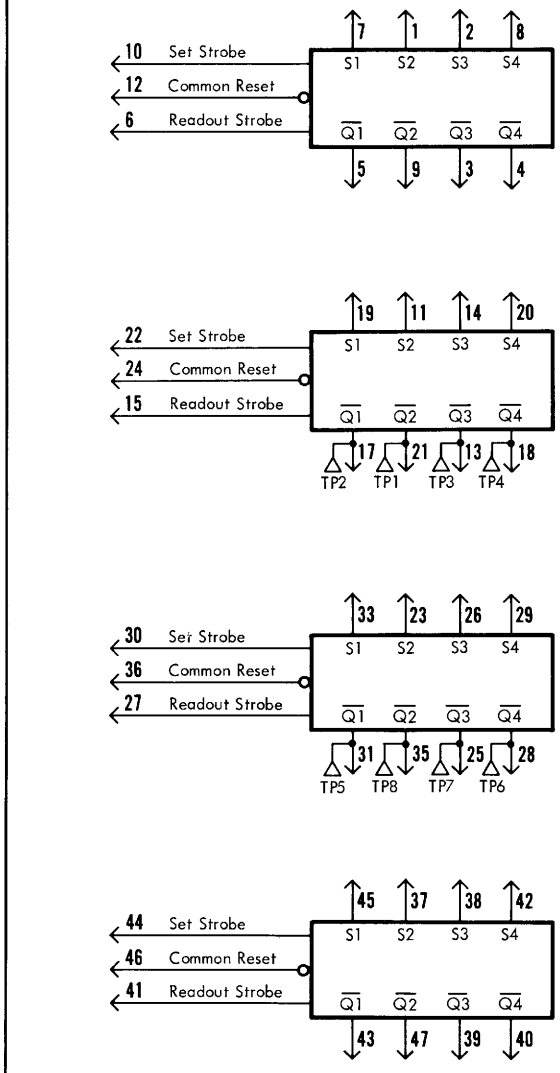
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			8
Input loading Data inputs Strobe and reset	units loads	 see logic diagram			 1 4
Timing, at 25°C, with loads of 15 pf	Data inputs must be stable for 28ns min., beginning at set strobe leading edge. Set strobe must be 28ns min in duration. Data is available 10ns (typ.) after readout strobe leading edge. Reset must be low for 28ns.				
+5 volt supply (Vcc)	ma			115	704*
Dissipation, per module	mw			576	3,870*

* at +5.5v and 20 MHz

PARTS LIST

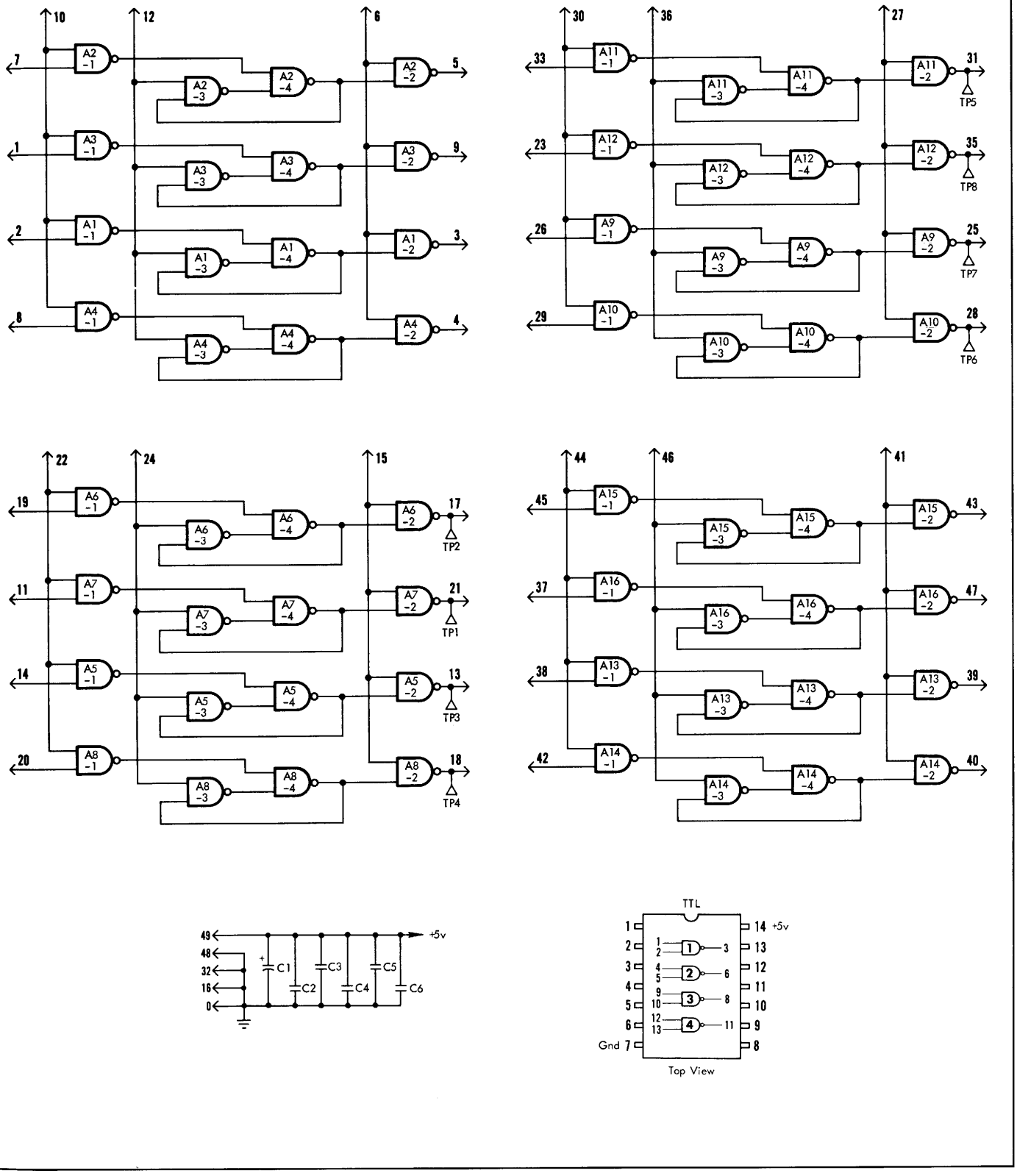
Designator	Description	Type	Qty.
A1 thru 16	IC gate, quad 2-in	9002	16
C1	Cap., tantalum 1μf		1
C2 thru 6	Cap., mylar, .01μf		5

LOGIC DIAGRAM



Polarizing keys 2 & 13

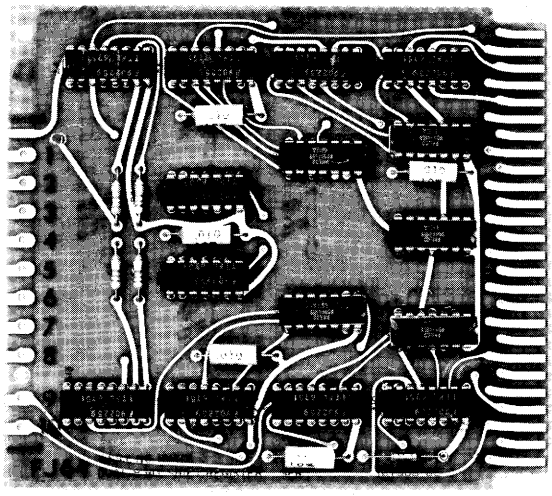
SCHEMATIC DIAGRAM, FJ63



FJ64
8-BIT SHIFT REGISTERS (TTL)

The FJ64 contains two independent 8-bit shift registers which can be used for serial-input to parallel-output, parallel-input to serial-output, or simple parallel-parallel storage. Common gated clock and reset inputs are provided. Strobed direct-set inputs, used for presetting, are also provided. A test point is provided at module front edge for each Q output of one register, and for Q7 and Q8 outputs of the other.

This module uses TTL circuits. Refer to FJ14 for DTL version.



SPECIFICATIONS

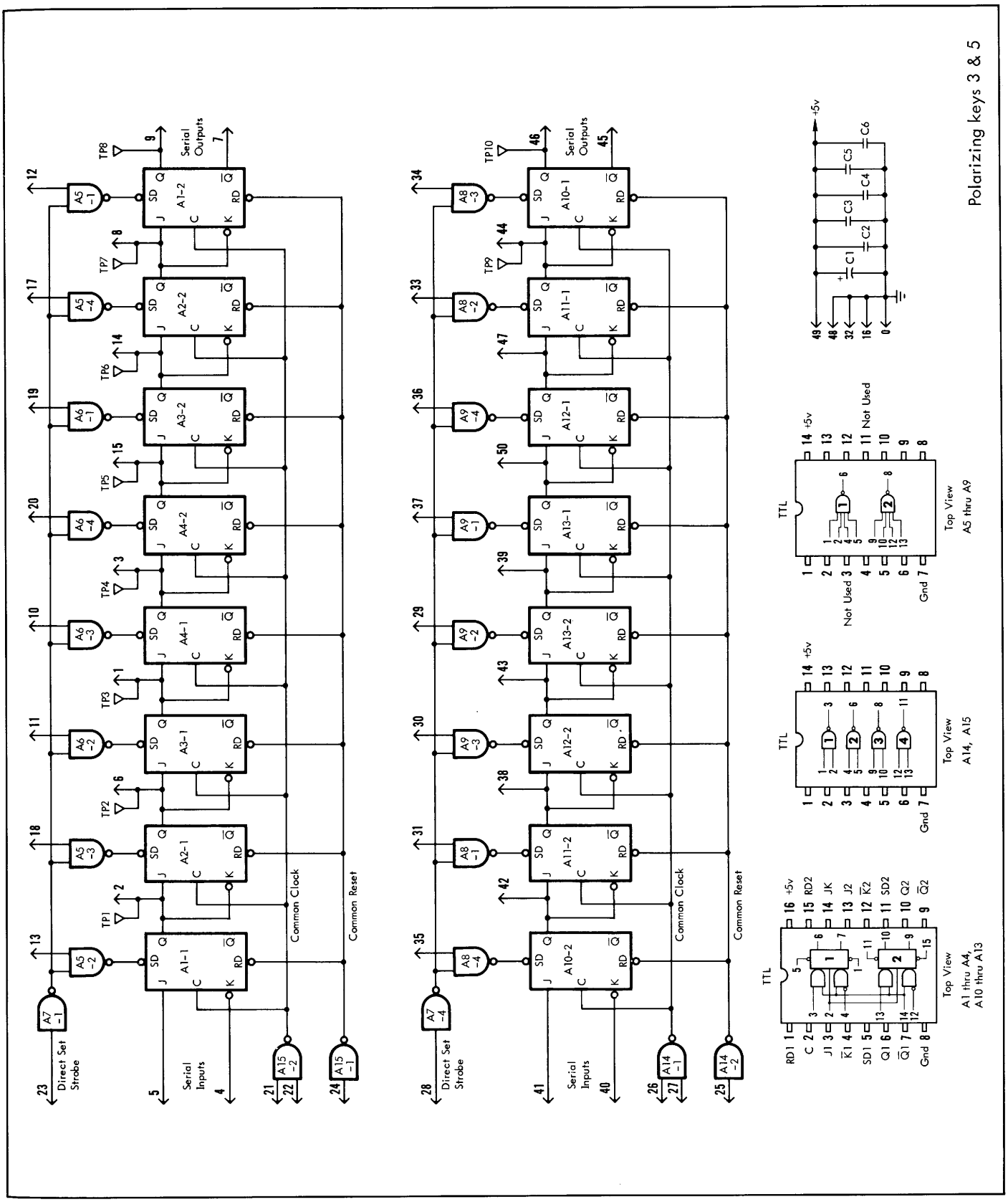
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	9, 7, 46, 45 all others			8 7
Input loading	unit loads	24, 21, 22, 25, 26, 27 all others			2 1
Propagation delay, at 25°C, with loads of 15 pf	ns			32	51
+5 volt supply (Vcc)	ma			296	758*
Dissipation, per module	watts			1.48	4.17*

* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 4, A12 thru 15	IC, flip-flop, dual	9022	8
A5, 6, 7, 10, 11	IC gate, quad 2-in	9002	5
A8, 9	IC, power gate	9001	2
C1	Cap., tantalum 1μf		1
C2, 3, 4	Cap., mylar .01μf		3

LOGIC DIAGRAM, FJ64



FJ66
BCD UP-COUNTER/DECODER (TTL)

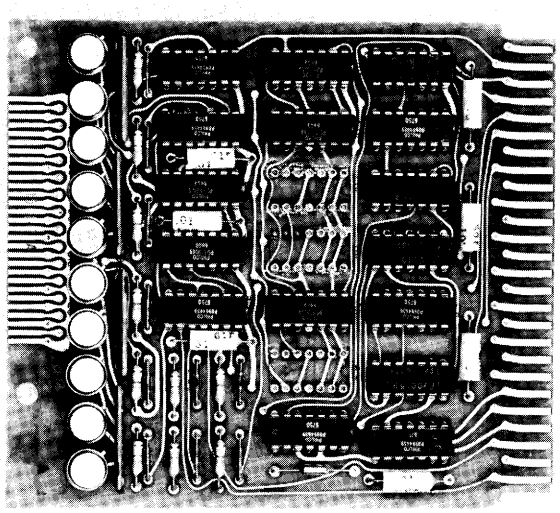
The FJ66 contains a 4-bit BCD ripple-through up-counter and a BCD to 10-line decoder. The decoder has both logic-level outputs and high current outputs which can be used to directly drive lamps or relays. The counter has strobed individual direct-set inputs for presetting, as well as a gated common reset line.

Certain terminals must be externally jumpered on the back plane, as shown in Table 1 in the logic diagram.

All three functions -- counting, 10-line decoding, and display driving -- are mounted on one module, reducing to one slot the mounting space required for one displayed decade.

The decoder-driver section is identical to the BJ60 module. The FJ66 uses the same general purpose etch pattern as the BJ60, BJ61, and FJ67 modules, filled with ICs as shown in the photograph at right.

The FJ66 uses TTL circuits. For a DTL version of this logic structure refer to FJ16.



SPECIFICATIONS

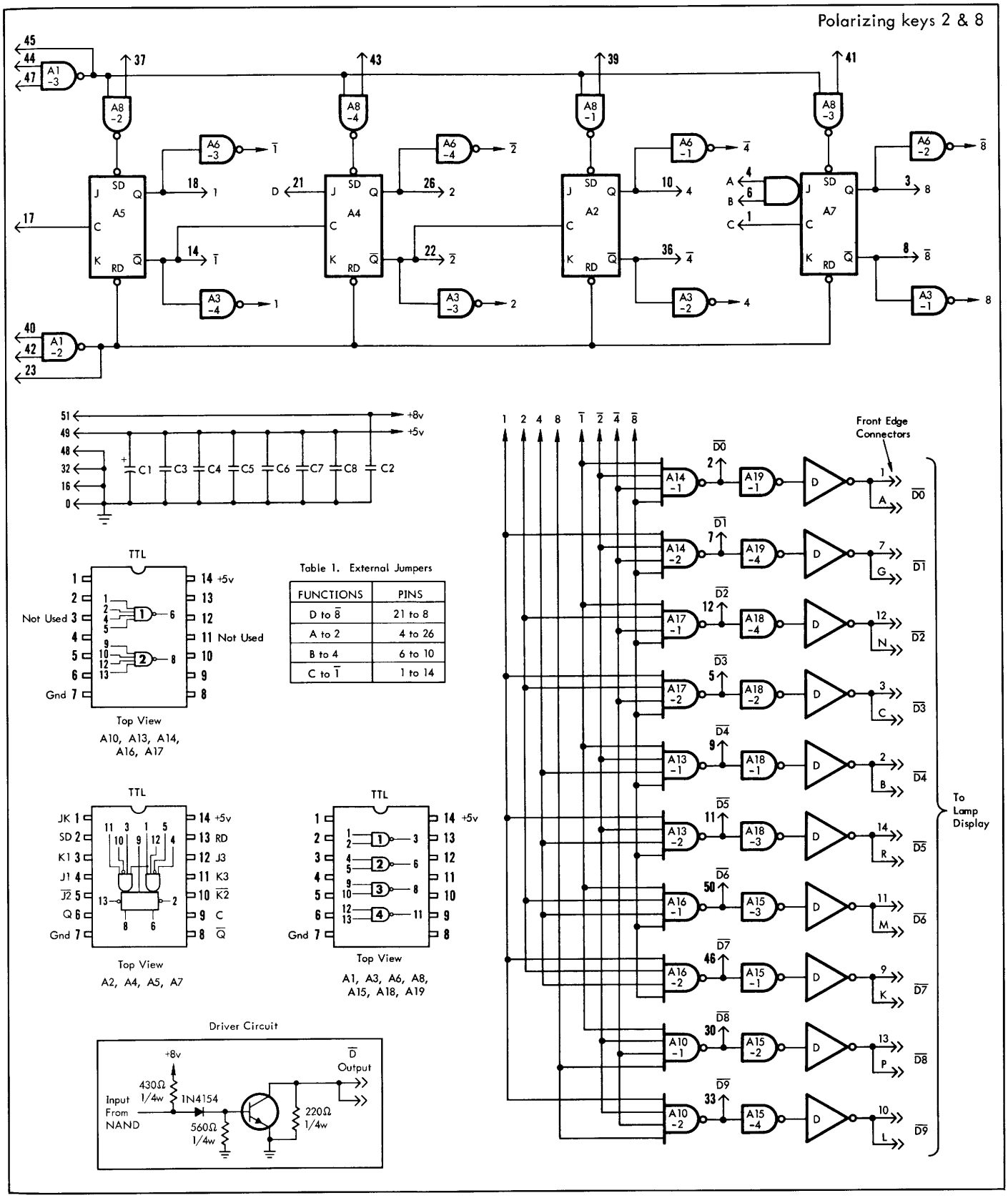
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL (at NAND outputs)	unit loads	18, 26, 10, 3 all others			6 7
Current per lamp driver (at 28 vdc max.)	ma	front edge			200
Keep-alive resistor (designed for use with 5v bulb; remove if v exceeds 8v)	ohms watts			220 1/4	
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 15 pf	ns			88	156
+5 volt supply (Vcc)	ma			121	486*
+8 volt supply	ma			198	216
Dissipation, per module	watts			2.19	4.58*

* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	Type	Qty.
A2, 4, 5, 7	IC, flip-flop single	9001	4
A1, 3, 6, 8, 15, 18, 19	IC gate, quad 2-in	9002	7
A9, 10, 11, 12, 13, 14, 16, 17	IC gate, dual 4-in	9004	8
A20, 21	Res. network, 220Ω, 1/4 w		2
A22, 23	Res. network, 560Ω, 1/4 w		2
R1 thru 10	Res., 430Ω, 1/4 w		10
CR1 thru 10	Diode	1N4154	10
Q1 thru 10	Transistor	2N3722	10
C2 thru 8	Cap., mylar, .01μf		7
C1	Cap., tantalum, 1μf		1

LOGIC DIAGRAM, FJ66



FJ67
BINARY UP-COUNTER WITH 16-LINE DECODER (TTL)

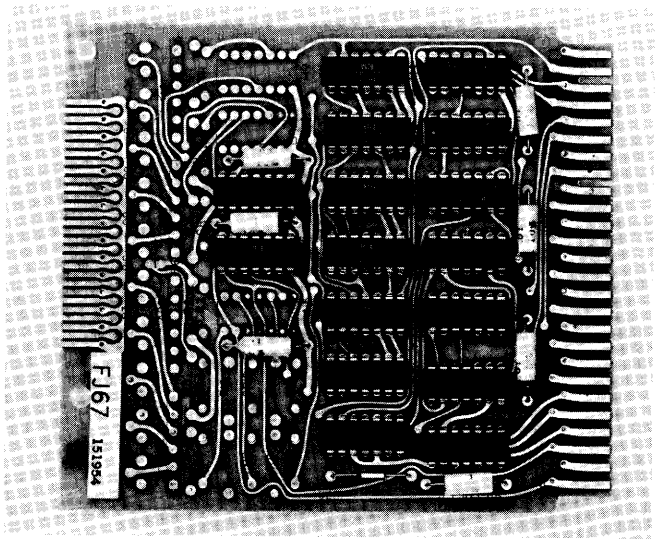
The FJ67 contains a 4-bit binary ripple-through up-counter and a binary to 16-line decoder. The counter has strobed individual direct-set inputs for presetting, as well as a gated common reset line.

Certain terminals must be externally jumpered on the back plane, as shown in Table 1 in the logic diagram.

Two functions -- counting and decoding -- are mounted on one module, providing extremely high packing density.

The decoder section is identical to the BJ61 module. The FJ67 uses the same general purpose etch pattern as the BJ61, BJ60, and FJ66 modules, filled with ICs as shown in the photograph below.

The FJ67 uses TTL circuits. For a DTL version of this logic structure refer to FJ17.



SPECIFICATIONS

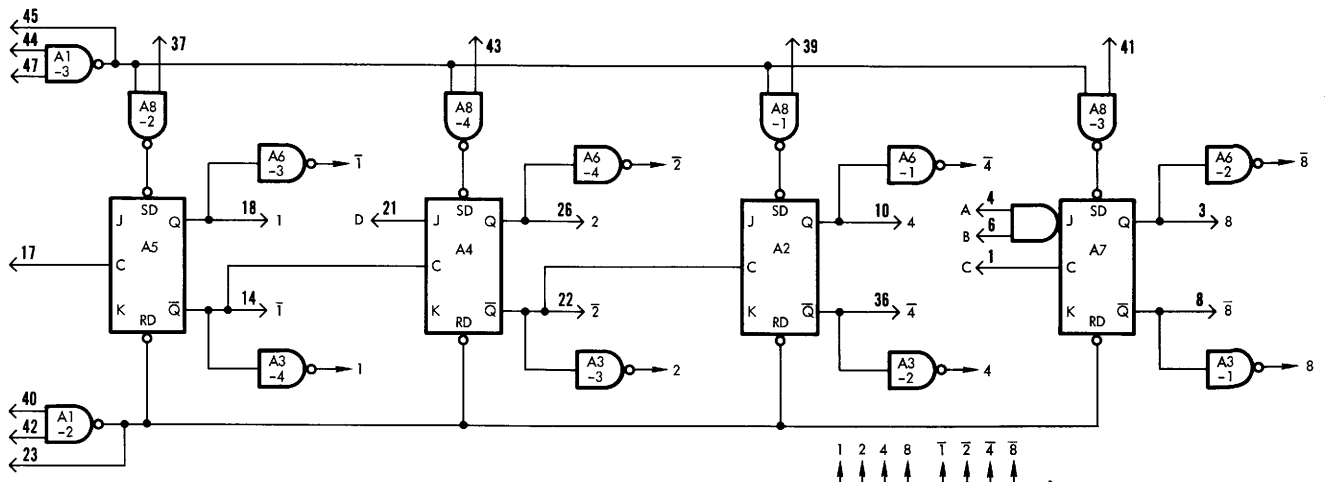
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	18, 26, 10, 3 14, 22, 36, 8 Decode outs.			5 7 8
Input loading	unit loads	clock inputs all others**			2 1
Propagation delay, at 25°C, with loads of 15 pf	ns			88	156
+5 volt supply (Vcc)	ma			108	440*
Dissipation, per module	mw			540	2,420*

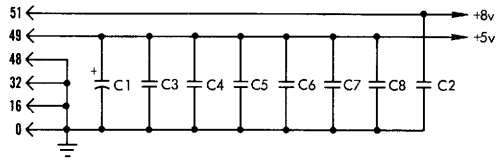
* at +5.5v and 20 MHz ** Do not use pins 23 & 45 as inputs

PARTS LIST

Designator	Description	Type	Qty.
A2, 4, 5, 7	IC flip-flop, single	9001	4
A1, 3, 6, 8	IC gate, quad 2-in	9002	4
A9, 10, 11, 12, 13, 14, 16, 17	IC gate, dual 4-in	9004	8
C2 thru 8	Cap., mylar, .01μf		7
C1	Cap., tantalum, 1μf		1

LOGIC DIAGRAM, FJ67





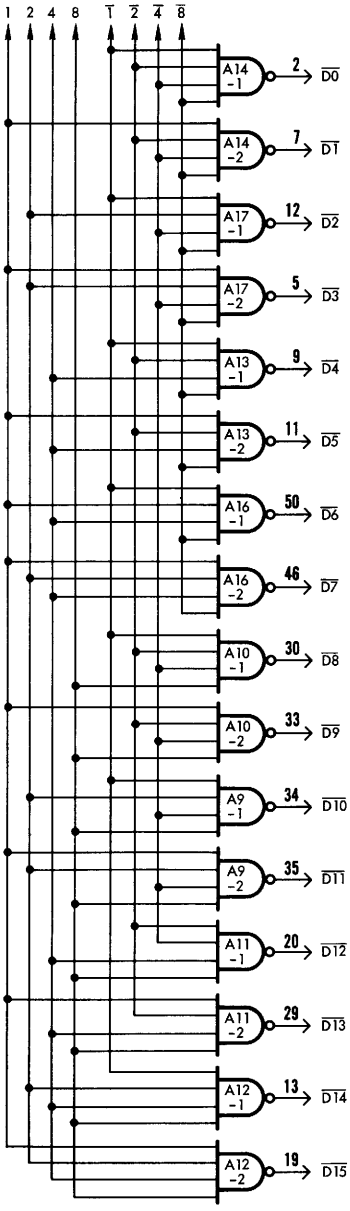
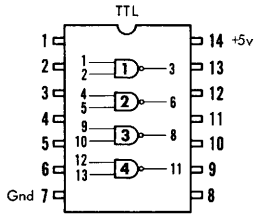
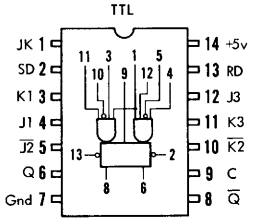


Table 1. External Jumpers

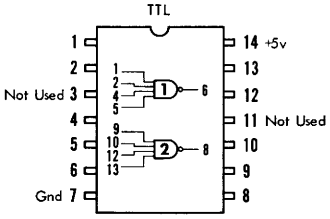
FUNCTIONS	PINS
A to $\overline{8}$	4 to 8
C to $\overline{4}$	1 to 36



Top View
A1, A3, A6, A8



Top View
A2, A4, A5, A7



Top View
A9 thru A14,
A16, A17

Polarizing keys 2 & 8

FJ68
BCD BIDIRECTIONAL COUNTER, 3 DECADES (TTL)

This module contains three identical decades of clocked BCD counting on one module. It functions as either up-counter or down-counter, depending on whether the control signals at pins 9, 25, and 41 are high (up) or low (down).

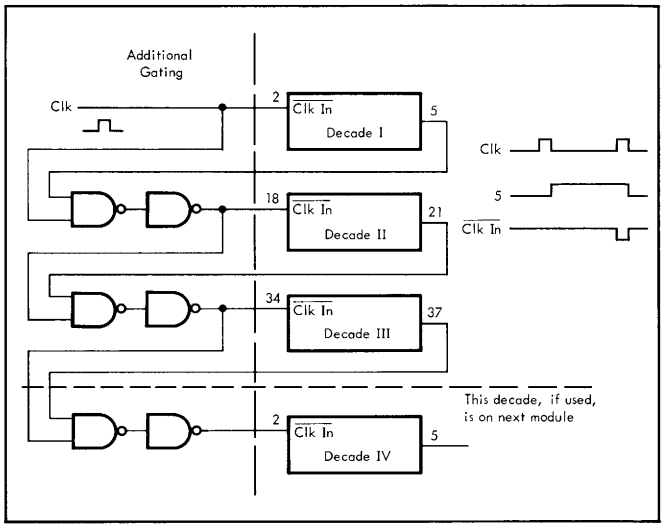
Common clock, common reset, and commonly strobed preset inputs are provided for each decade.

Each decade has a clock output (pins 5, 21, 37) which is used to provide clock input to the next decade, when two decades are serially chained together. If counting direction is to remain stable, each clock output can connect directly to next clock input. However, if up/down changeover during counter operation is anticipated, additional gating (shown in diagram at right) is required to prevent possible loss of data.

Front-edge test points are provided at the Q outputs of ten of the twelve counter flip-flops.

This module uses TTL circuits. A DTL version of a similar logic structure is the FJ18.

The FJ68 interfaces conveniently with the BJ62.



Gating Required For Dynamic Up/Down Transition

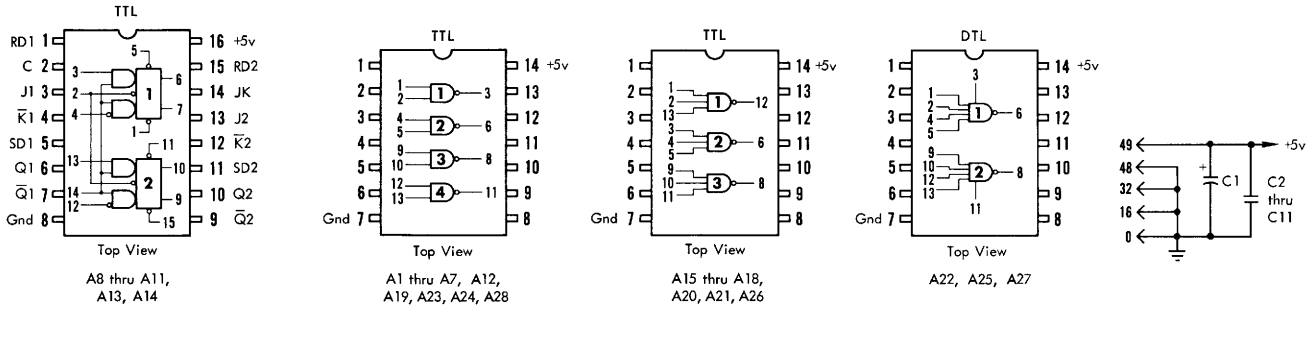
SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	1, 17, 33 all others			6 7
Input loading	unit loads				1
Propagation delay, at 25°C, with loads of 15 pf	ns			37	60
+5 volt supply (Vcc)	ma			299	1056*
Dissipation, per module	watts			1.50	5.81*

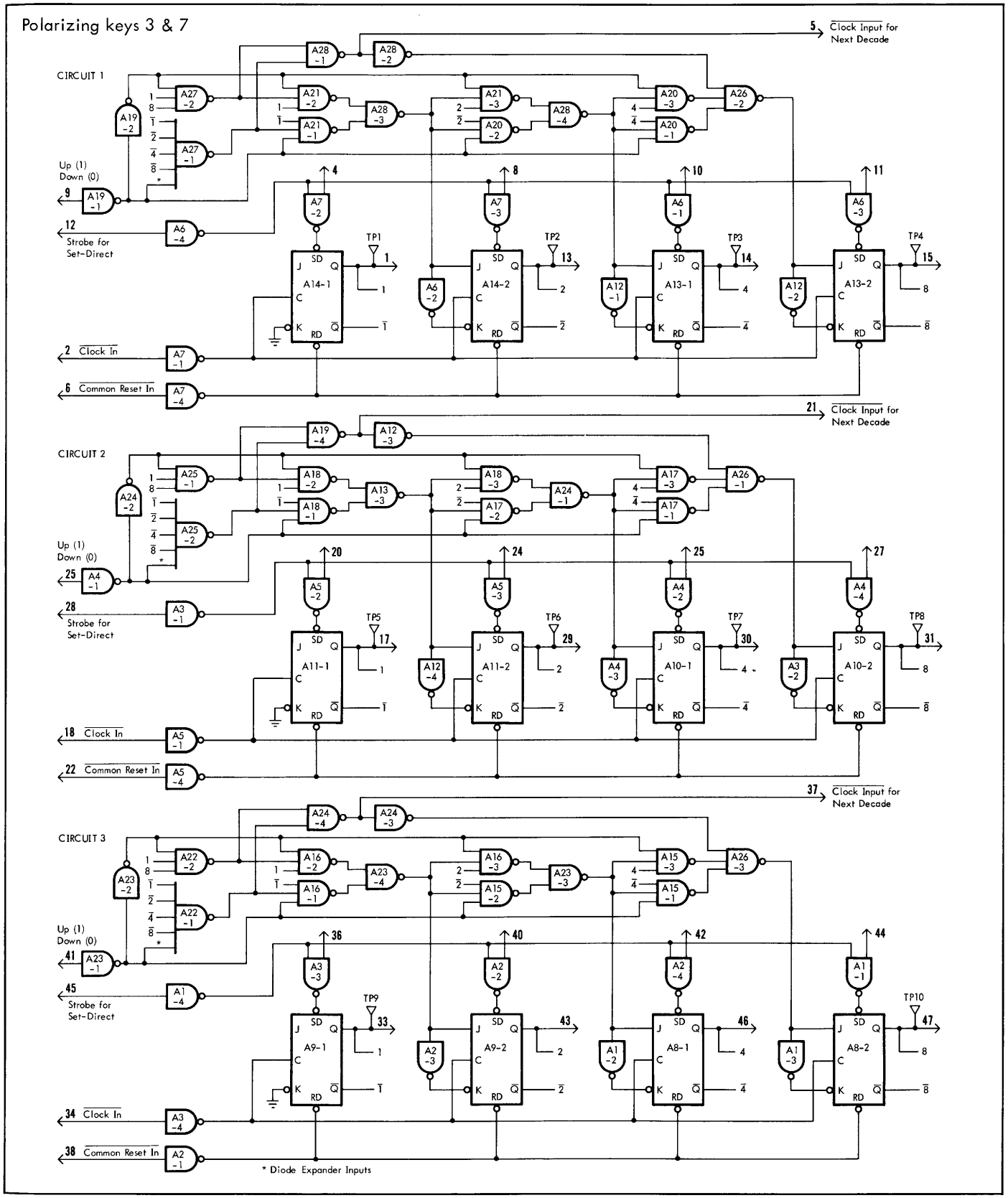
* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	Type	Qty.
A22, 25, 27	IC gate, dual 4-in	9004	3
A8, 9, 10, 11, 13, 14	IC flip-flop, dual	9022	6
A1 thru 7, 19, 12, 23, 24, 28	IC gate, quad 2-in	9002	12
A15, 16, 17 18, 20, 21, 26	IC gate, triple 3-in	9003	7
CR1	Diode	1N4154	3
C2 thru 11	Cap., mylar, .01μf		10
C1	Cap., tantalum, 1μf		1



LOGIC DIAGRAM, FJ68



HT58
UNIVERSAL OPERATIONAL AMPLIFIER

The HT58 is a fast, high-input impedance, high-output current, differential amplifier with provisions for adjustment of gain and zero offset. In addition, the input offset voltage temperature coefficient is adjustable.

A feature of the amplifier is a front-end shield plane, driven from the common mode point, and an electrical "FET Guard", which reduces the effective input capacity when used in the buffer mode. Pins adjacent to the inputs are also driven to eliminate effects of stray capacitance. This signal may be used for external guards if desired.

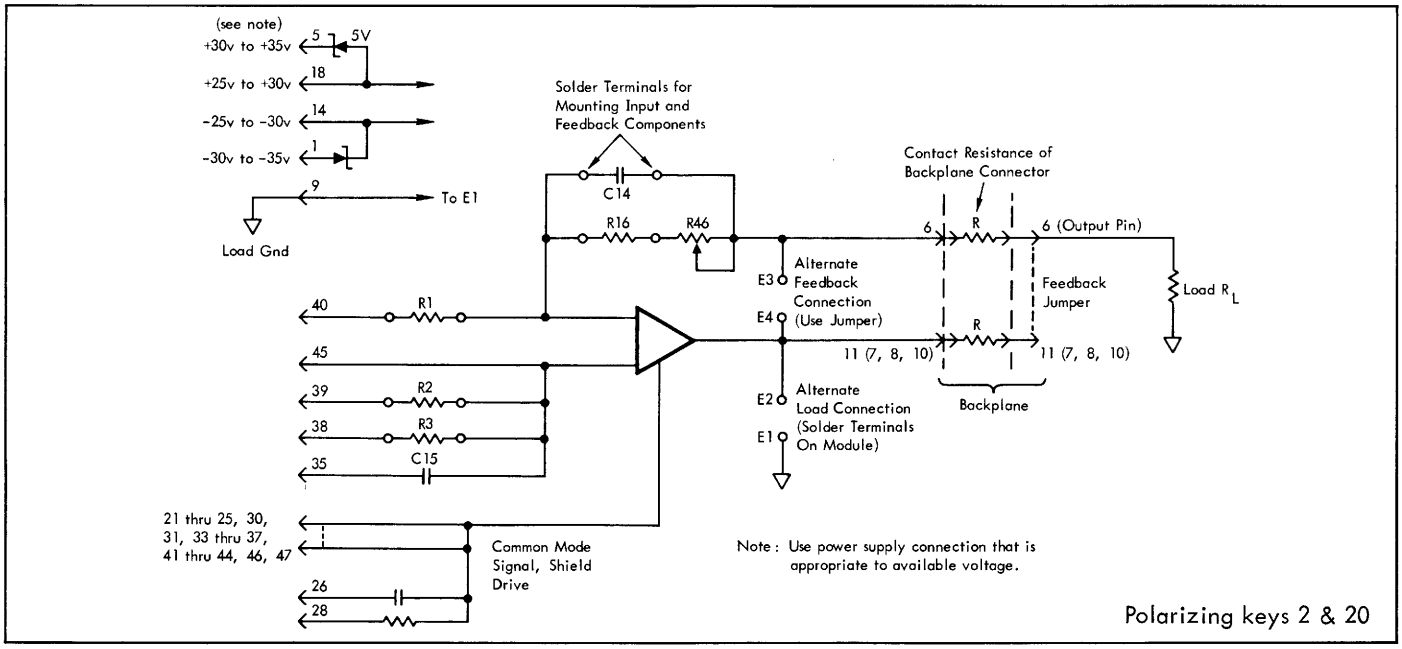
The amplifier is available in a variety of popular gain configurations (see Tables 1, 2, 3). Other resistor configurations may be obtained on special request. In addition, a unit is available without gain resistors or gain pot.

For detailed circuit schematic and parts list request HT58 data sheet.

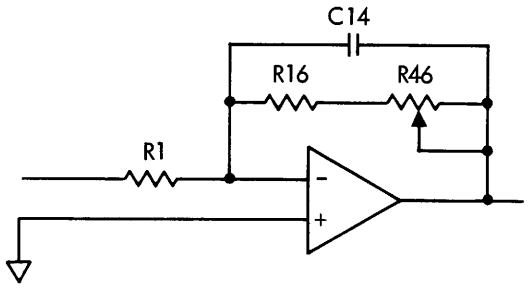
SPECIFICATIONS

Input	
Open loop gain:	$.5 \times 10^6$
Gain accuracy:	.01% with precision feedback
Linearity:	.01% with precision feedback
Common mode rejection:	100 db, dc; 60 db, 1 KHz (Resistor error may be adjusted out)
Input impedance (buffer mode):	Junction FET typically paralleled by less than 1 pf capacitance
Input bias current (FET leakage)	.1 nanoamp at 25°C; 1 n.a. at 55°C
Input voltage range:	±10 volts divided by the closed loop gain (min. 1, max. 10)
Recovery time from 10X overvoltage: (not to exceed common mode of ±15v on either input)	Op Amps and Diff. Amp: 10 µsec Buffer: 12 µsec.
Output	
Voltage swing:	±10 volts
Current:	±40 ma. (self limiting)
Output impedance:	.01 ohm max. at D.C., all configurations; 1 ohm max. at 1 MHz, unity gain (proportional to gain)
Min. load impedance:	250 ohms 2,000 pf
Settling time to within 1 mv of final value:	5 µsec, at unity gain, full load (+10v to -10v or -10v or +10v)
Slew rate:	10v/µsec., typical
Noise (Wideband):	.5 mv. p-p RTO
Output connections:	Either at solder terminals on board or at connector pin (with feedback jumpered). See General Configuration.
Power Supply Voltage:	Pins 18 & 14, +(25 thru 30)v and -(25 thru 30)v; or pins 5 and 1, +(30 thru 35)v and -(30 thru 35)v
Power Supply Current:	25 ma. plus load current
Power Supply Recommended:	PT24

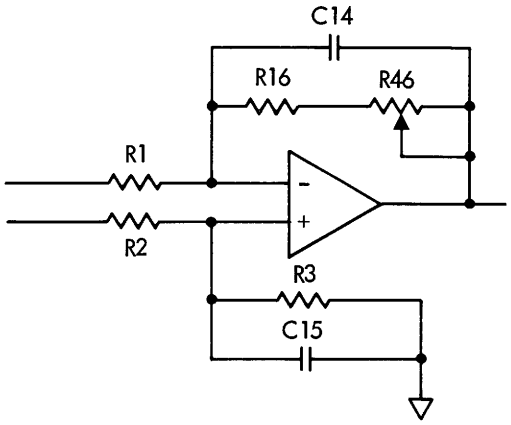
GENERAL CONFIGURATION



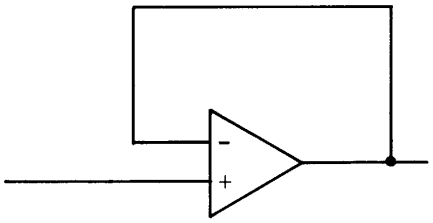
Operational Amplifier



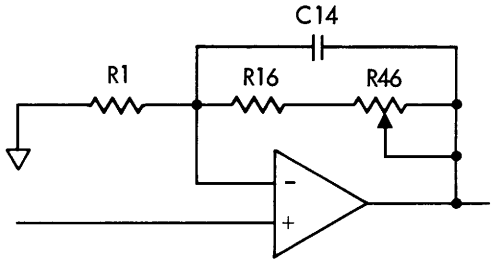
Differential Amplifier



Unity Gain Buffer



Buffer With Gain



Popular Gain Configurations, HT58

Table 1. Operational Amp. Configurations

④ Dash No.	R1	R16 + R46	① C14	R2	R3	Gain	Settling Time ② µsecs
-1	10K	10K	10PF	-	-	X1	5
-2	10K	100K	5PF	-	-	X10	10
-3	100K	100K	5PF	-	-	X1	10
-4	Short	2.5K	10PF	-	-	③	5

Table 2. Differential Amp. Configurations

Dash No.	R1	R16 + R46	C14	R2	R3	Gain	Ts
-5	10K	10K	10PF	10K	10K	X1	5
-6	10K	100K	5PF	10K	100K	X10	10
-7	100K	100K	5PF	100K	100K	X1	10
-8	-	-	-	-	-	-	-

Table 3. Buffer Configurations

Dash No.	R1	R16 + R46	C14	R2	R3	Gain	Ts
-9	-	-	Short	-	-	X1	5
-10	1K	9K	10PF	-	-	X10	10

① May be tailored for specific applications.

② 20v swing on output, settling to within 1 mv of final value.

③ ±4 ma input current produces $\overline{+}$ 10v output.

④ Order configuration desired by dash no. suffix. Example: HT58-6 is second configuration listed in Table 2.

HT72
GENERAL PURPOSE OPERATIONAL AMPLIFIERS

The HT72 contains two general purpose operational amplifier circuits, designed for applications not requiring the performance of the HT58 amplifier. This module uses two integrated circuit linear amplifiers, with additional components, which provide two major improvements:

1. Additional power amplification produces greater output current (20 ma at 10v).
2. An internal supply voltage control allows broader tolerance in supply voltage (±20%). The internal voltage control assures that gain is stable in spite of supply voltage changes.

Differential or unipolar input may be used. Output is single-ended. Configurations available are similar to those of the HT58 module (refer to HT58 description). Due to the excellent gain stability, accuracy of the amplifier depends primarily on feedback resistor accuracy. The amplifier is provided with 1% feedback resistors, mounted on standoff terminals, which result in overall accuracy better than 1.4%. If these are replaced with 0.01% resistors, at user option, accuracy will be better than 0.1%.

Additional standoff terminals are provided on the module, which allow the user to modify the feedback of the amplifier by adding components.

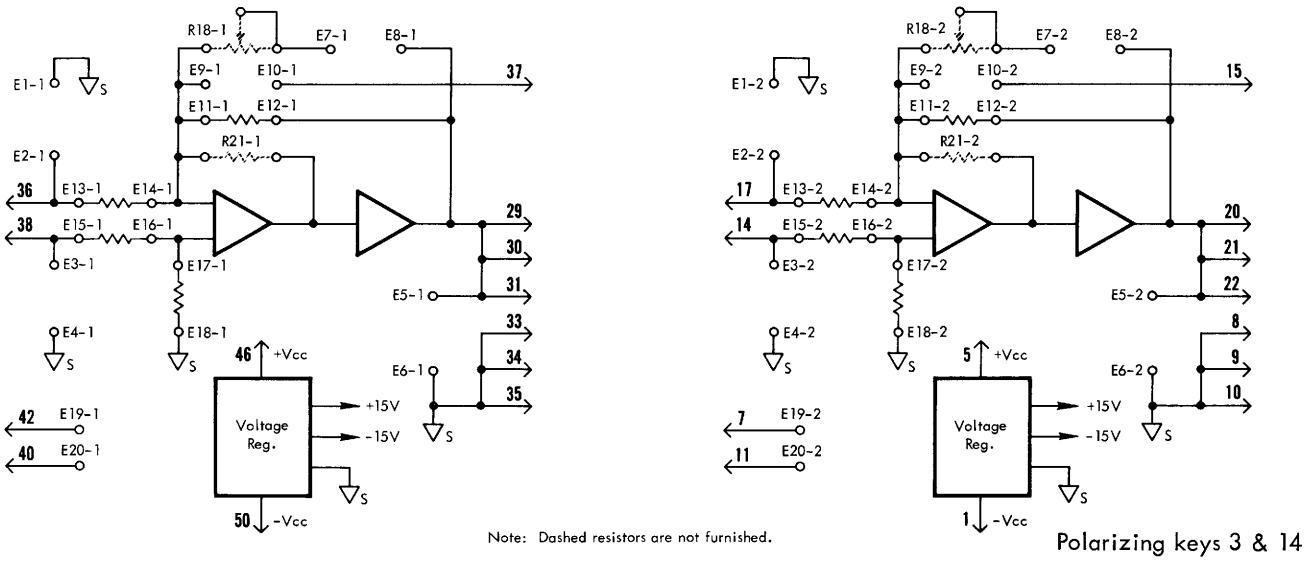
For detailed schematic diagram and parts list, request HT72 data sheet.

SPECIFICATIONS

Characteristic	Units	Min.	Typ.	Max.
Input				
Open loop gain		12,000	45,000	
Temp. coefficient of input offset voltage*	μv/°C		6	
Input impedance	Kohms	150	400	
Input bias current	μamp.		0.5	2.0
Input offset current	nanoamp.		100	750
Input voltage range	volts			±10
Differential input voltage range	volts			±5.0
Output				
Voltage swing	volts			±10
Current	ma			20
Output impedance (open loop)	ohms	22	30	50
Power supply voltage	volts	20	25	30
Power supply current	ma	25		90
Dissipation, per module	watts	0.50		2.7

* The total offset of the amplifier is adjustable to within ±300 μvolts.

GENERAL CONFIGURATION



Note: Dashed resistors are not furnished.

Polarizing keys 3 & 14

HT73
VOLTAGE COMPARATORS

The HT73 module contains nine independent logic circuits with differential inputs. When the voltage at the + input becomes more positive than the voltage at the - input by a predetermined comparison value the output goes to logic 1 (high) level. The comparison level is determined by the resistor and Vref connections which are made at the - input.

The HT73 is used as a sensitive level detector or interface module. The HT73 uses the same circuit board and amplifiers as the AT69 differential receiver.

Comparator sensitivity is better than 10 mv; that is, when the + input becomes 10 mv more positive than the comparison level, the output goes high. The comparison level is the voltage at point P (see connection diagram).

The voltage at comparison point P is usually determined by the combination of V ref and a voltage divider network R3/R5 that can be placed at the - input. The resistor R3 that is provided on the module is a 4.64K ohm, 1% precision resistor. R5 is supplied by the user.

The voltage at the comparison point, P, should not go beyond the range -5v to +5v when supply voltages of ±8v are used for -v and +v. The range at point P can be extended as far as -12v to +12v by raising -v and +v to -15v and +15v.

This voltage divider arrangement permits the use of a relatively high precision reference voltage such as the 35 volts that is available from the WT49 module.

An external variable comparator level input may be substituted as shown in the connection diagram, if an adjustable comparison input is available.

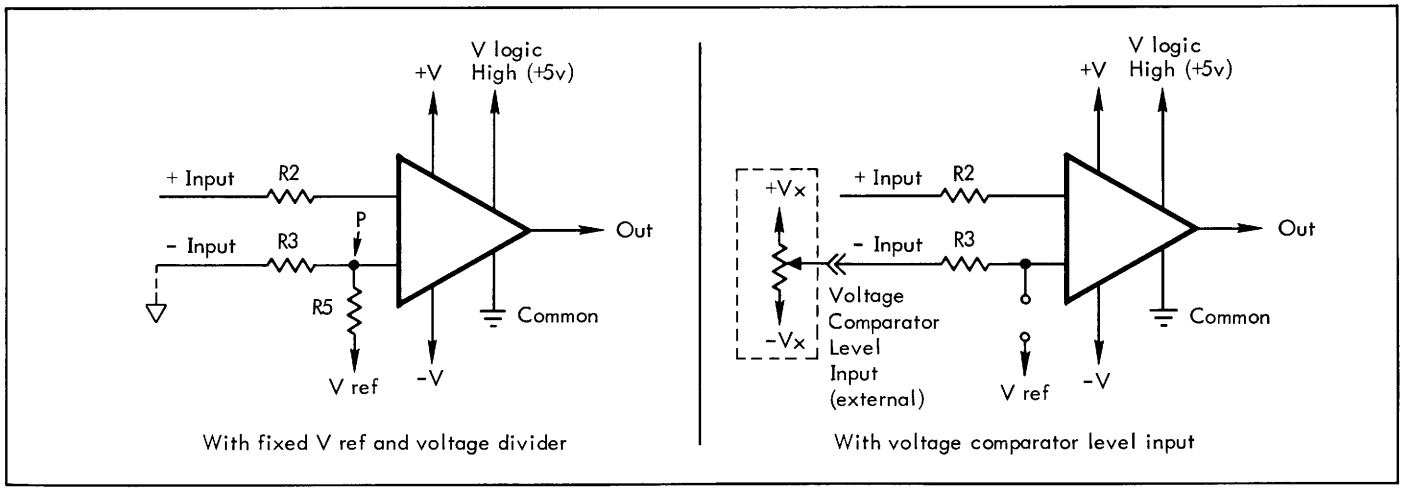
The HT73 output logic level is determined by the supply voltage connected to pin 26. For J Series use pin 26 is tied to +5 volts.

Both input terminals and the Vref terminal are available at front-edge cable connectors (⟶») as well as at back-panel connectors (⟶).

SPECIFICATIONS

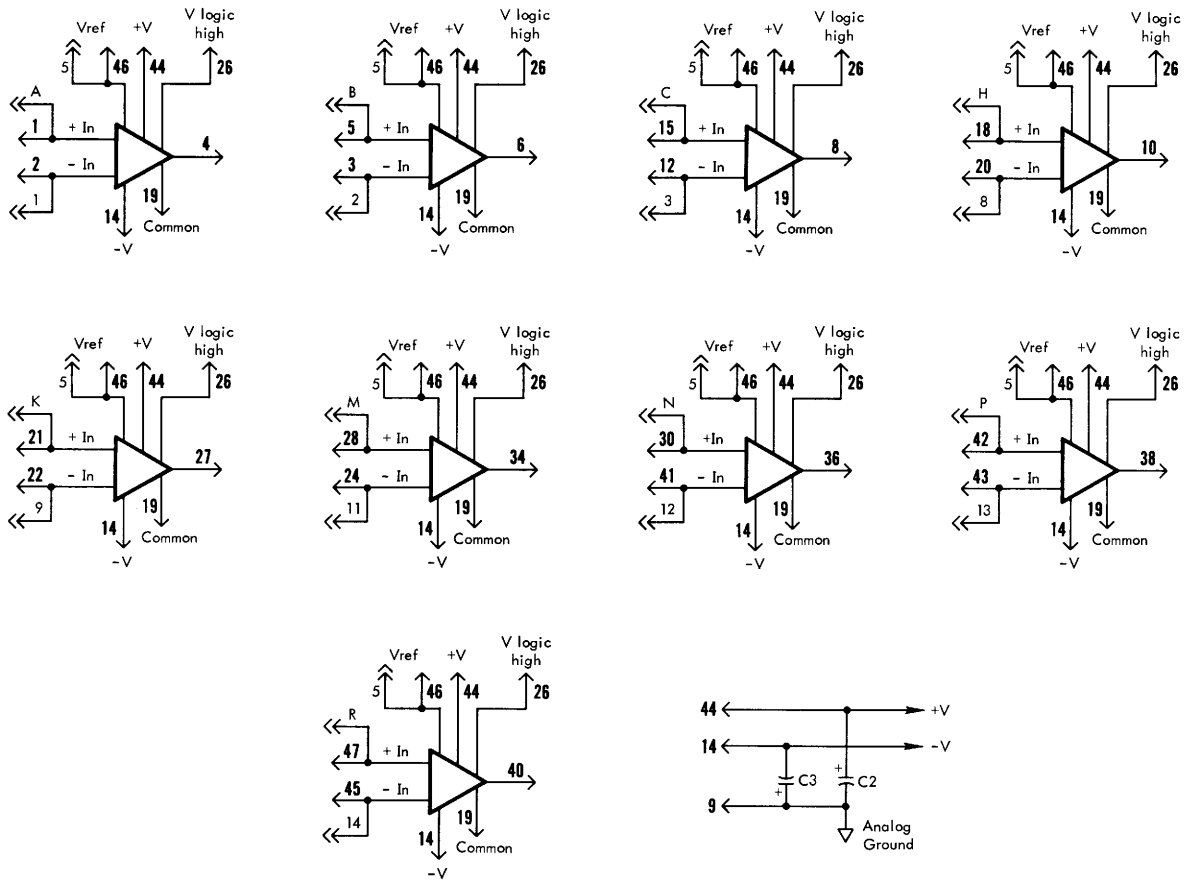
Characteristic	Units	Min.	Typ.	Max.
Data rate	MHz			1
Max. input voltage (from + input to ground)	volts			15
Comparison level range (at point P)				
with +v=+8v and -v=-8v	volts	-5		+5
with +v=+15v and -v=-15v	volts	-12		+12
Vref	Max. value depends on R3 and R5 (refer to text)			
Input impedance	ohms	200K		
Output logic 1 level	volts	4.5		5.5
Output logic 0 level	volts	0		0.4
Fan-out, into DTL	unit			37
Fan-out, into TTL	loads			30
Propagation delay, at 25°C	ns		170	
+5 volt supply (Vcc)	ma		76	85
+8 volt supply	ma		220	270
-8 volt supply	ma		16	25
Dissipation, per module	watts		2.27	3.07*

* at 10% overvoltage



HT73 Connection Diagram

LOGIC DIAGRAM, HT73



Polarizing keys 3 & 13

The IJ10 module contains sixteen independent gate circuits. Fourteen are connected as 2-input NANDs, which perform the function $Q = \overline{A \cdot B}$. The other two circuits are connected as inverters. An unwired input functions as if it were wired True.

If the negative-True logic convention is assumed (low level, 0v, is True) then the gates can be considered NORs, which perform the function $Q = \overline{A + B}$. In either case any unused inputs may be left unwired.

The gate outputs can be connected in parallel to form wired logic functions.

The IJ10 uses DTL circuits. Refer to IJ60 for a TTL version.

SPECIFICATIONS

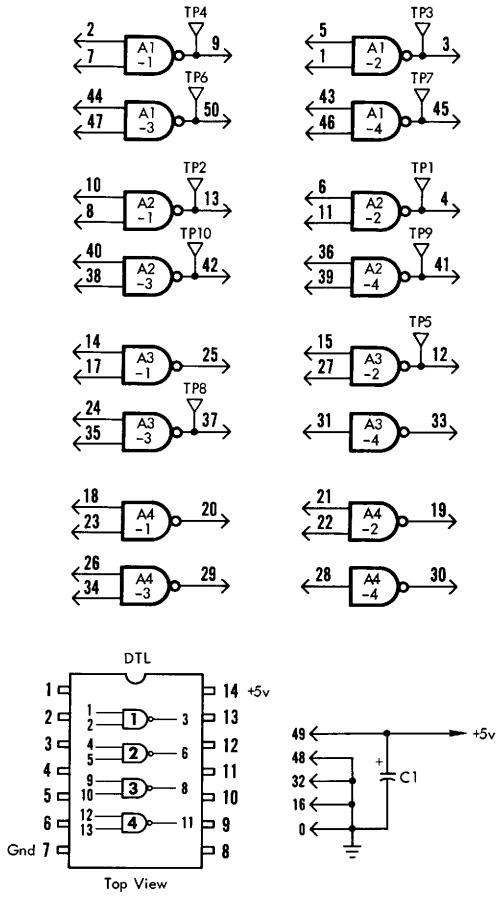
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			31	51
+5 volt supply (Vcc)	ma			28.8	40.3*
Dissipation, per module	mw			144	222*

*at +5.5v

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 4	IC gate, quad 2-in	946	4
C1	Cap. mylar, .01μf		1

LOGIC DIAGRAM



Polarizing keys 2 & 6

IJ11
3-INPUT, 4-INPUT NANDS (DTL)

The IJ11 module contains six 4-input NAND gates and four 3-input NAND gates, which perform the function $Q = \overline{ABCD}$ and $Q = \overline{ABC}$ respectively. An unwired input functions as if it were wired True.

If the negative True logic convention is assumed (low level, 0v, is True) then the gates can be considered NORs, which perform the function $Q = \overline{A + B + C + \text{etc.}}$

In either case any unused inputs may be left unwired.

The gate outputs can be connected in parallel to form wired logic functions.

The IJ11 uses DTL circuits. Refer to IJ61 for a TTL version.

SPECIFICATIONS

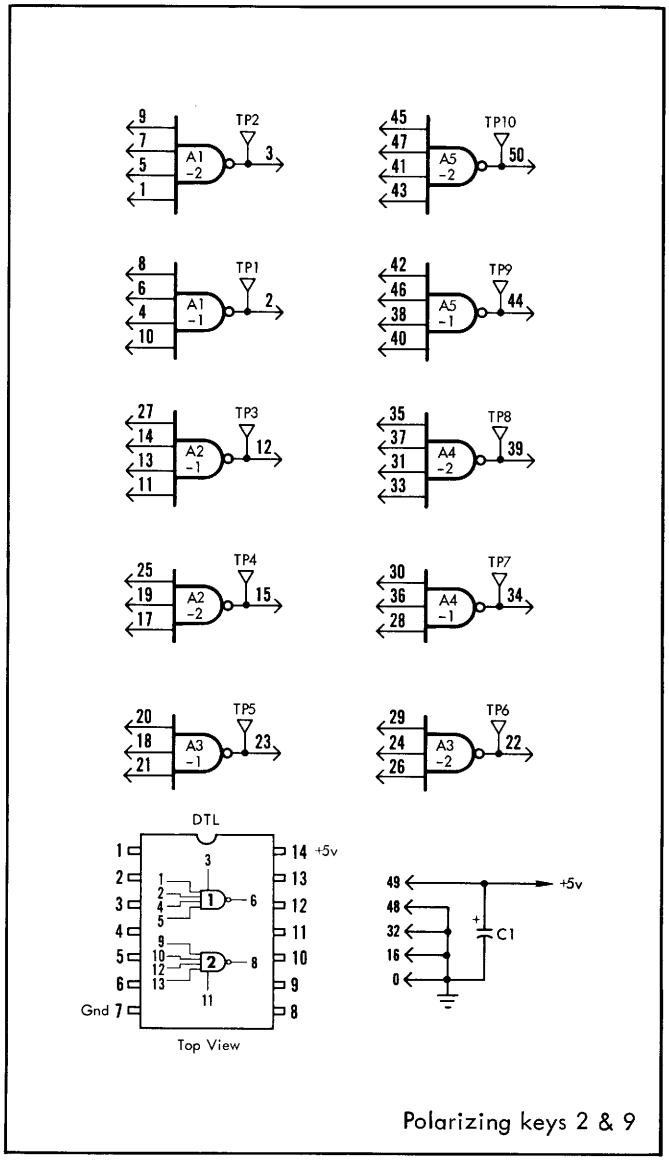
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			31	51
+5 volt supply (Vcc)	ma			18	25.2*
Dissipation, per module	mw			90	138.5*

* at +5.5v

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 5	IC gate, dual 4-in	930	5
C1	Cap. mylar, .01µf		1

LOGIC DIAGRAM



The IJ12 module contains fourteen inverters and six 2-input NAND gates. The 2-input NANDs perform the function $Q = \overline{AB}$. An unwired input functions as if it were wired True.

If the negative-True logic convention is assumed (low level, 0v is True) then the gates can be considered NORs, which perform the function $Q = \overline{A} + \overline{B}$. In either case any unused inputs may be left unwired.

The gate or inverter outputs can be connected in parallel to form wired logic functions.

The IJ12 uses DTL circuits. For a TTL version refer to IJ62.

SPECIFICATIONS

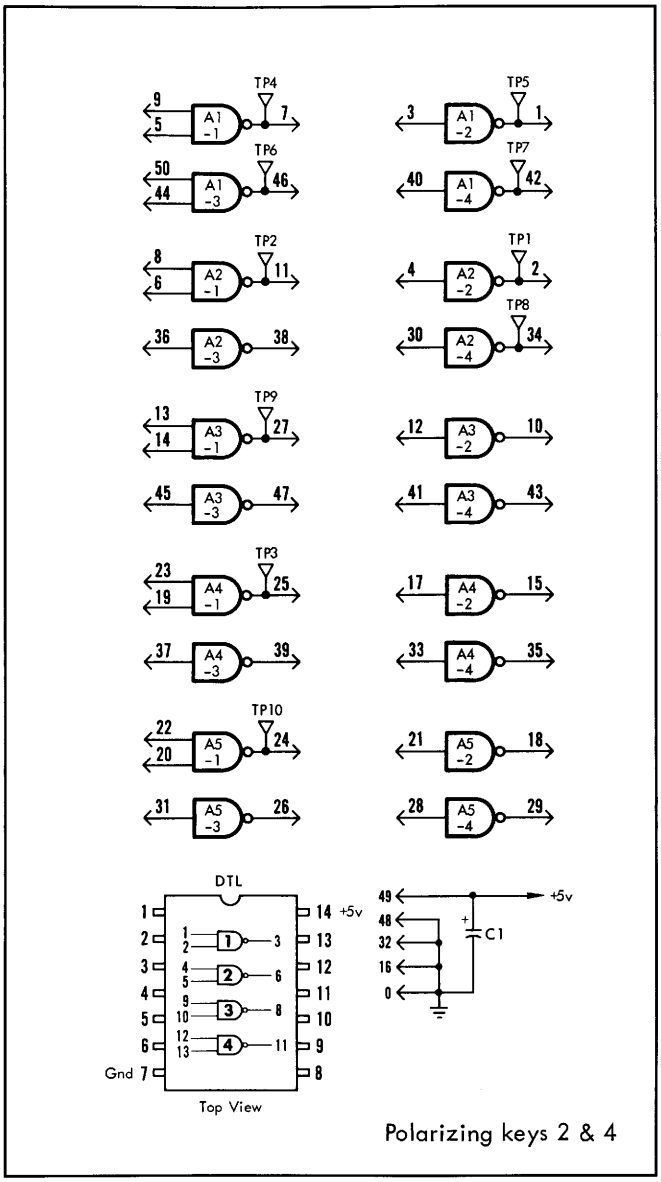
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 0 level Logic 0 level	volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			31	51
+5 volt supply (Vcc)	ma			36	50.4*
Dissipation, per module	mw			180	277*

*at +5.5v

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 6	IC gate, quad 2-in	946	6
C1	Cap. mylar, .01μf		1

LOGIC DIAGRAM



IJ13
2-INPUT POWER NANDS (DTL)

The IJ13 module contains sixteen power NANDs arranged in pairs with a strobe input common to each pair. Two independent 2-input power NANDs are also provided. Type 944 DTL power gates are used, with an external 1.1K ohm (3 unit load) pull-up resistor connected to each gate output. (The resistors are on the module).

Wired logic functions can be formed by wiring outputs together. Subtract three unit loads from the basic driving capability of 22 unit loads for each output added to the wired-logic node: D = 22-3n, where D is the drive capability in unit loads, and n is the number of outputs wired together.

If inputs as well as outputs are wired together, there is no loss of drive capability due to addition of outputs in parallel. In this case the drive capability is additive (contrary to the wired-logic case) because all gates are at all times in the same state when inputs are connected in parallel. To obtain total driving capability in unit loads, multiply the number of gates wired in parallel by 22.

The IJ13 is particularly useful for driving clock lines or other high current loads whose timing must be closely controlled to avoid logic races.

For a DTL module with active pull-ups and the same logic configuration refer to IJ14. For a TTL version refer to IJ64.

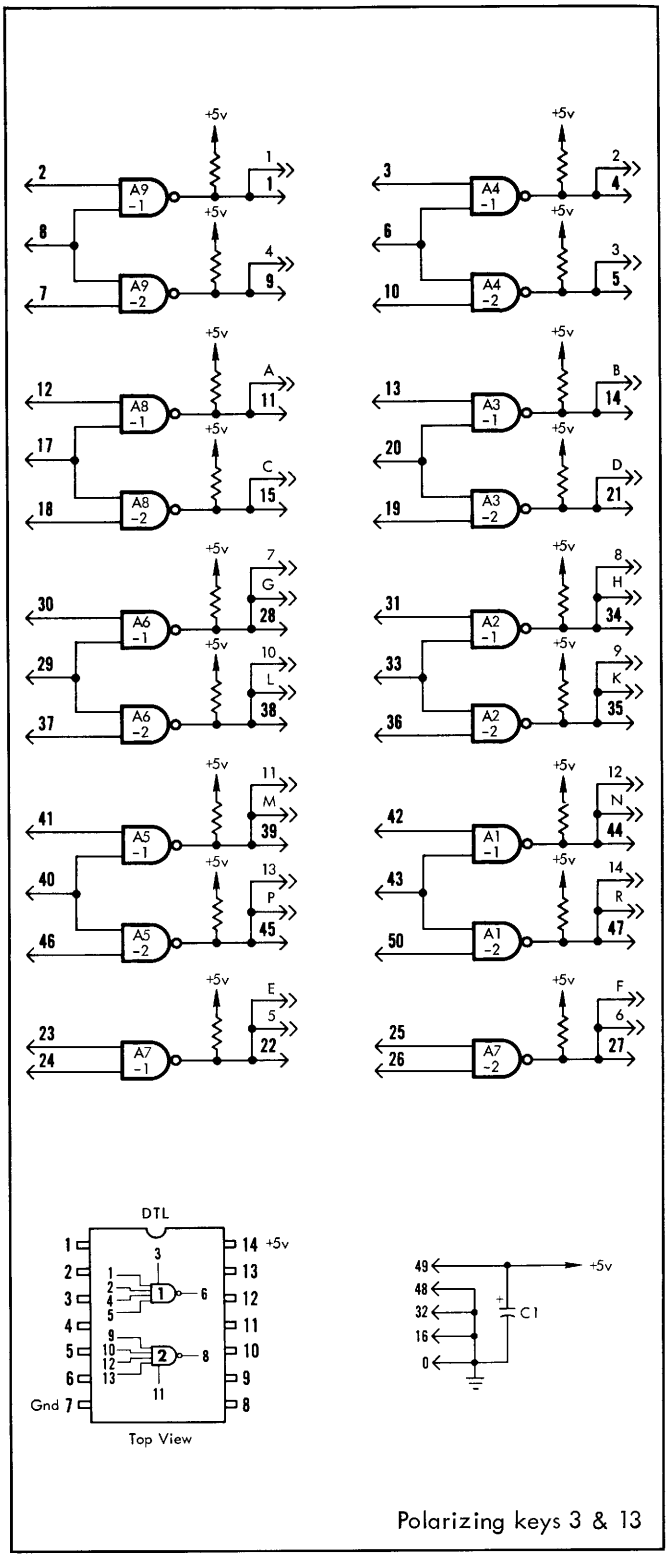
SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			22
Input loading	unit loads	all inputs			1
Propagation delay at 25°C, with loads of 125Ω/100 pf	ns			36	56
+5 volt supply (Vcc)	ma			113.6	138
Dissipation, per module	mw			567.9	759.0

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 9	IC, power gate	944	9
R1 thru 18	Res. 1.1KΩ, 1/4w		18
C1	Cap. mylar, .01μf		1

LOGIC DIAGRAM



The IJ14 module contains sixteen power NANDs arranged in pairs with a strobe input common to each pair. Two independent 2-input power NANDs are also provided. Type 932 DTL power gates are used. These gates have "active pull-ups" similar to the output circuits found in TTL, although the input circuits use diodes as in DTL. A pull-up resistor is placed on the chip in series with a transistor which conducts only in the logic 1 (high) state. No external pull-up resistor is required. The output impedance in the logic 1 state is very low, on the order of 150 ohms, which leads to high capacitive drive capability and consequently a fast rise time.

Wired logic functions are not allowed with this type of output. If wired logic is desired, use the IJ13 module.

However, when inputs of several gates are paralleled, their outputs may also be connected, in order to create one driver with greater fan-out than is available from a single power NAND. In this case the connection of several outputs to a single common point is legitimate because with the inputs connected in parallel all gates are at all times in the same state. Therefore all outputs will also be at all times in the same state, and the dissipation rating of the output transistors on the IC chips will not be exceeded. To obtain total fan-out capability in unit loads, multiply the number of parallel gates by 25.

The IJ14 is particularly useful as a DTL to TTL interface because it combines a DTL input with an active pull-up output. Use IJ14 for fanout (into TTL) greater than four. The low output impedance also makes it a good driver for high capacitance loads such as ribbon cable. For a TTL version see IJ64.

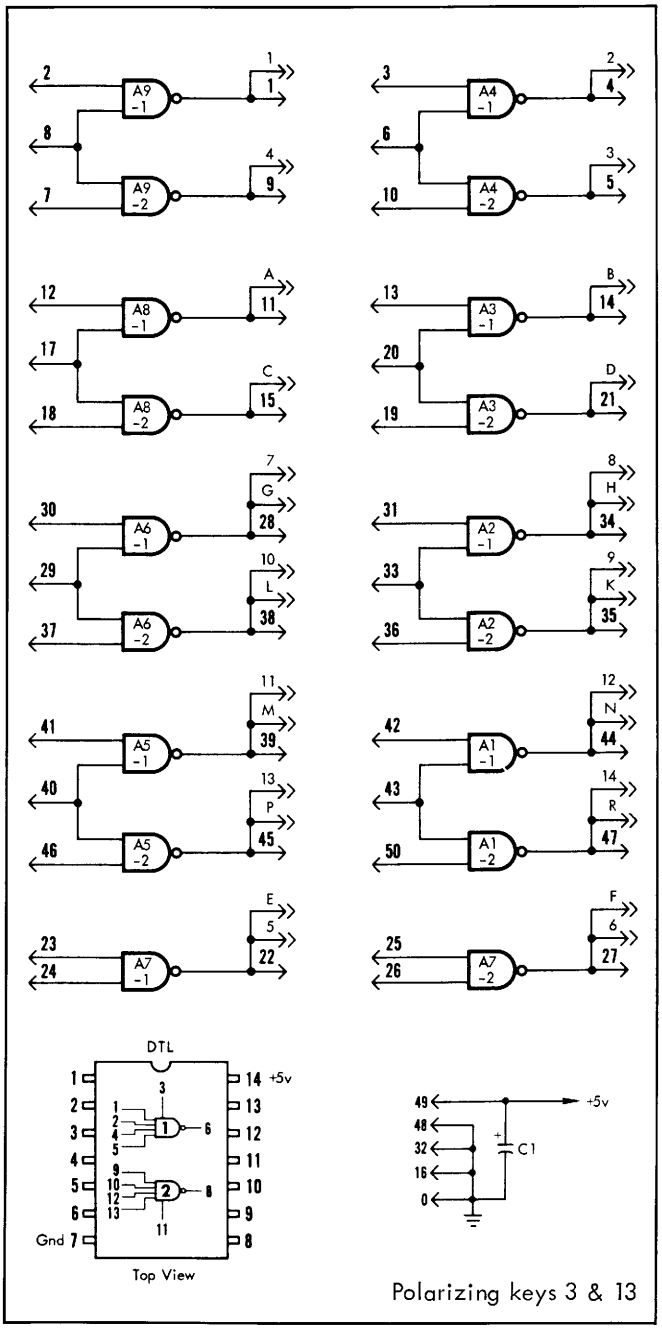
SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			25
Input loading	unit loads	all inputs			1
Propagation delay at 25°C with loads of 125Ω/100 pf	ns			41	61
+5 volt supply (Vcc)	ma			107	119.5
Dissipation, per module	mw			532	657.4

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 9	IC, power gate	932	9
C1	Cap. mylar, .01μf		1

LOGIC DIAGRAM



IJ16
4-INPUT POWER NANDS (DTL)

The IJ16 module contains six power NANDs arranged in pairs with a strobe input common to each pair. Four independent power NANDs are also provided. Type 932 DTL power gates are used. These gates have "active pull-ups" similar to the output circuits found in TTL, although the input circuits use diodes as in DTL. A pull-up resistor is placed on the chip in series with a transistor which conducts only in the logic 1 (high) state. No external pull-up resistor is required. The output impedance in the logic 1 state is very low, on the order of 150 ohms, which leads to high capacitive drive capability and consequently a fast rise time.

Wired logic functions are not allowed with this type of output. If wired logic is desired, use the IJ15.

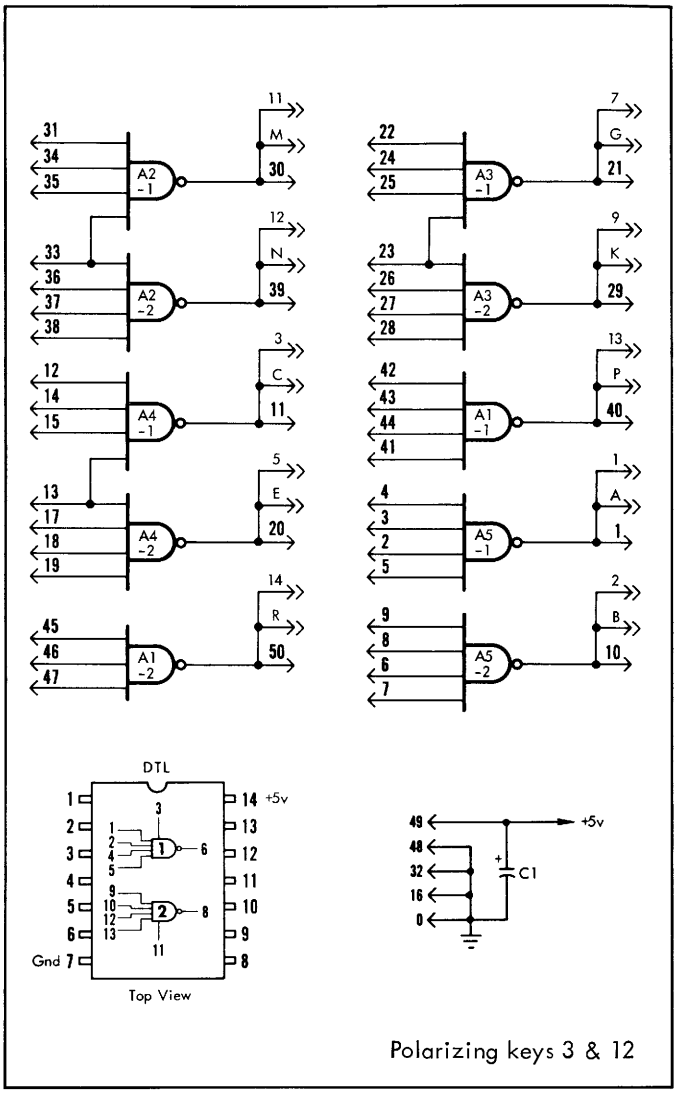
However, when inputs of several gates are paralleled, their outputs may also be connected, in order to create one driver with greater fan-out than is available from a single power NAND. In this case the connection of several outputs to a single common point is legitimate because with the inputs connected in parallel all gates are at all times in the same state. Therefore all outputs will also be at all times in the same state, and the dissipation rating of the output transistors on the IC chips will not be exceeded. To obtain total fan-out capability in unit loads, multiply the number of parallel gates by 25.

The IJ16 is particularly useful as a DTL to TTL interface because it combines a DTL input with an active pull-up output. Use IJ16 for fanout (into TTL) greater than four. The low output impedance also makes it a good driver for high capacitance loads such as ribbon cable. For a TTL version see IJ66.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			25
Input loading	unit loads	all inputs			1
Propagation delay at 25°C, with loads of 125Ω/100 pf	ns			41	61
+5 volt supply (Vcc)	ma			59	66.4
Dissipation, per module	mw			295	365

LOGIC DIAGRAM



Polarizing keys 3 & 12

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 5	IC, power gate	932	5
C1	Cap. mylar, .01μf		1

The IJ60 module contains sixteen independent gate circuits. Fourteen are connected as 2-input NANDs, which perform the function $Q = \overline{A \cdot B}$. The other two circuits are connected as inverters. An unwired input functions as if it were wired True.

If the negative-True logic convention is assumed (low level, 0v, is True) then the gates can be considered NORs, which perform the function $Q = \overline{A + B}$. In either case any unused inputs may be left unwired.

The gate outputs cannot be connected in parallel to form wired logic functions.

The IJ60 uses TTL circuits. For a DTL version, refer to IJ10.

SPECIFICATIONS

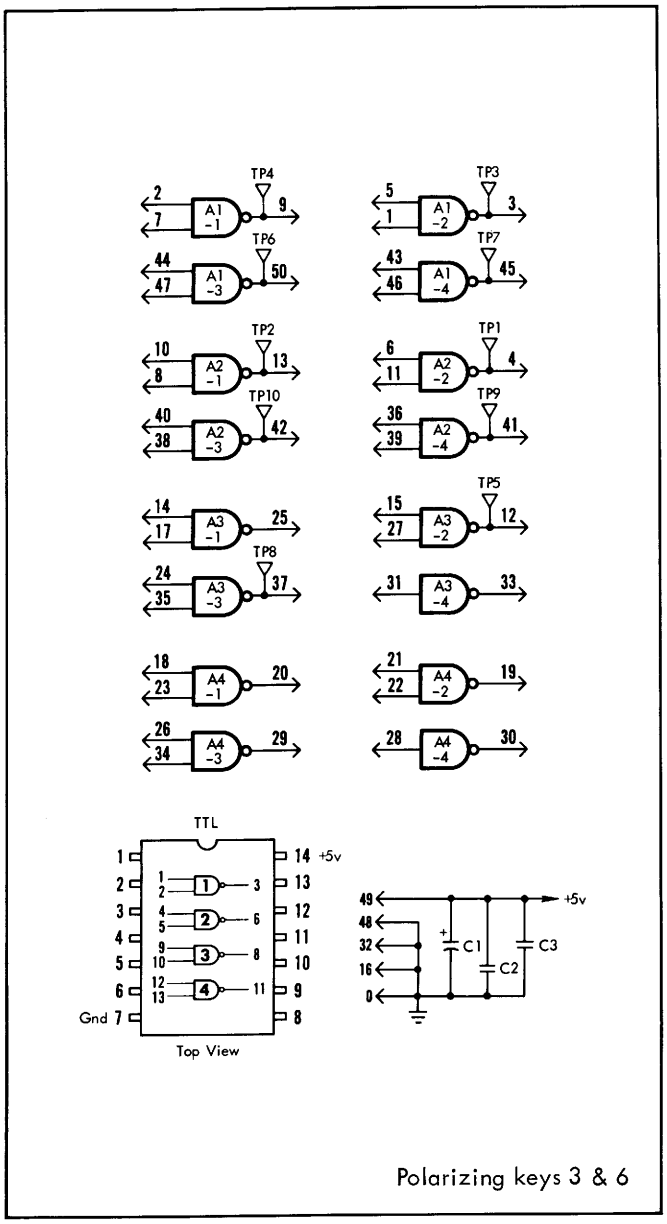
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 15pf	ns			10	14
+5 volt supply (Vcc)	ma			28.8	176*
Dissipation, per module	mw			144	968*

*at +5.5v and 20 MHz

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 4	IC gate, quad 2-in	9002	4
C1	Cap. tantalum, 1μf		1
C2, 3	Cap. mylar, .01μf		2

LOGIC DIAGRAM



IJ61
3-INPUT, 4-INPUT NANDS (TTL)

The IJ61 module contains six 4-input NAND gates and four 3-input NAND gates, which perform the function $Q = \overline{ABCD}$ and $Q = \overline{ABC}$ respectively. An unwired input functions as if it were wired True.

If the negative True logic convention is assumed (low level, 0v, is True) then the gates can be considered NORs, which perform the function $Q = \overline{A + B + C}$ + etc.

In either case any unused inputs may be left unwired.

The gate outputs cannot be connected in parallel to form wired logic functions.

The IJ61 uses TTL circuits. Refer to IJ11 for a DTL version.

SPECIFICATIONS

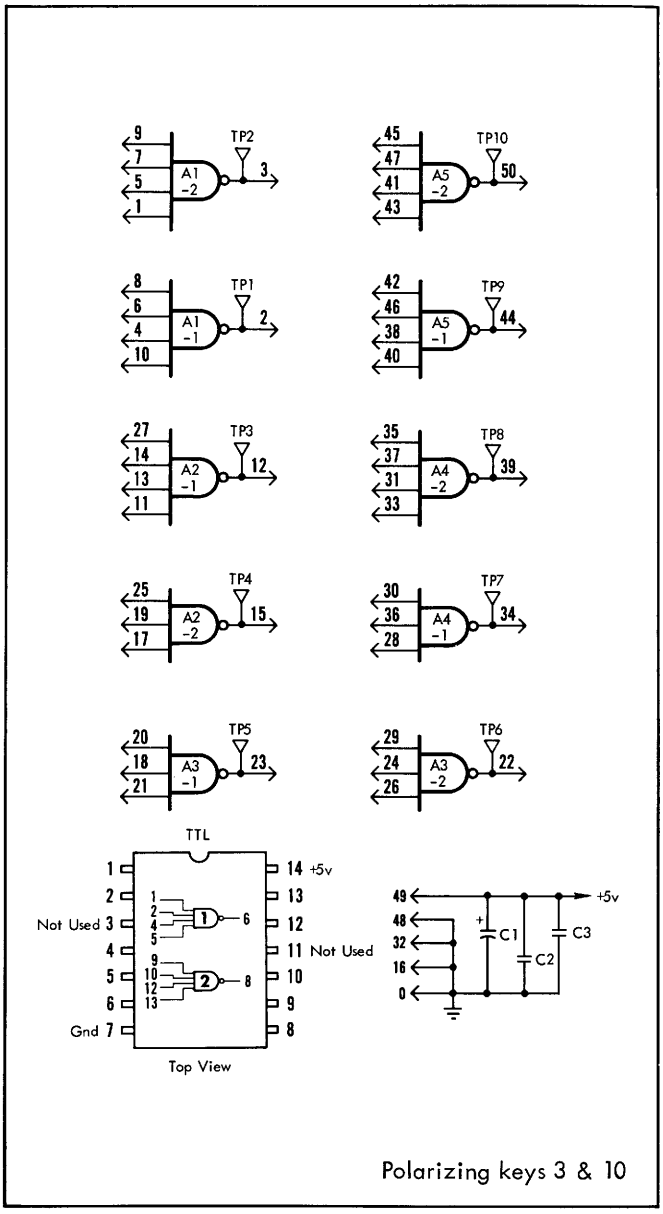
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 15pf	ns			10	14
+5 volt supply (Vcc)	ma			18	110*
Dissipation, per module	mw			90	605*

* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 5	IC gate, dual 4-in	9004	5
C1	Cap. tantalum, 1μf		1
C2, 3	Cap. mylar, .01μf		2

LOGIC DIAGRAM



Polarizing keys 3 & 10

The IJ62 module contains fourteen inverters and six 2-input NAND gates. The 2-input NANDs perform the function $Q = \overline{AB}$. An unwired input functions as if it were wired True.

If the negative-True logic convention is assumed (low level, 0v, is True) then the gates can be considered NORs, which perform the function $Q = \overline{A} + \overline{B}$. In either case any unused inputs may be left unwired.

The IJ62 uses TTL circuits. For a DTL version refer to IJ12.

SPECIFICATIONS

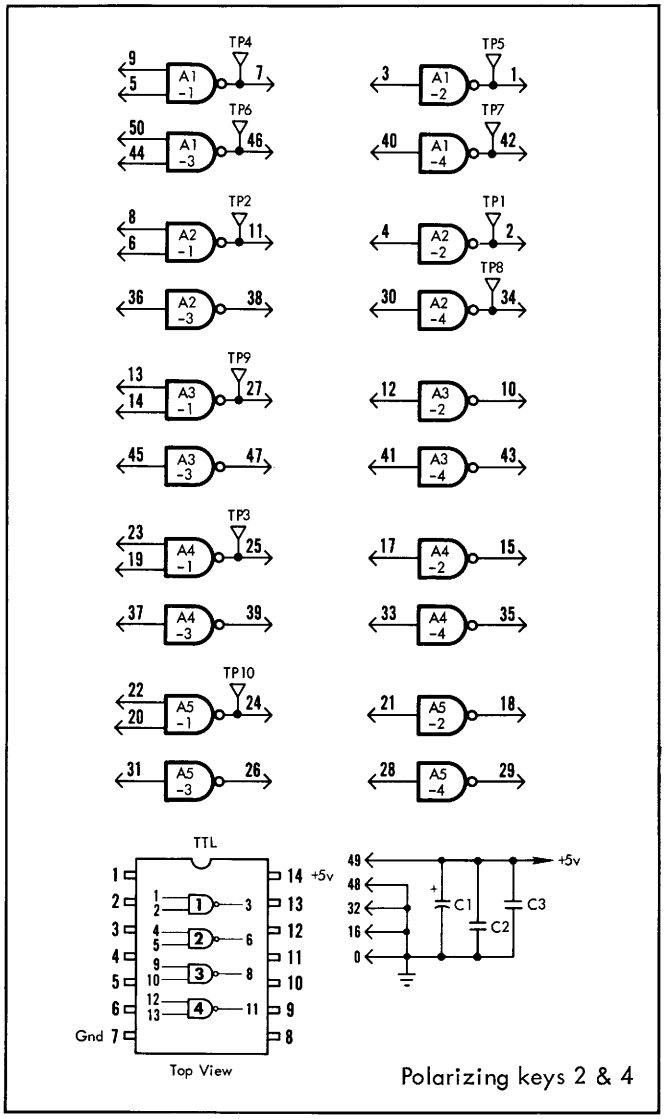
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 15pf	ns			10	14
+5 volt supply (Vcc)	ma			36	220*
Dissipation, per module	mw			180	1,210*

*at +5.5v and 20 MHz

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 6	IC gate, quad 2-in	9002	6
C1	Cap. tantalum, 1µf		1
C2, 3	Cap. mylar, .01µf		2

LOGIC DIAGRAM



IJ64
2-INPUT POWER NANDS (TTL)

The IJ64 module contains sixteen power NANDs arranged in pairs with a strobe input common to each pair. Two independent 2-input power NANDs are also provided. The power gates used have multiple-emitter inputs and "active pull-up" outputs as is usually the case with TTL circuits.

The output impedance in the logic 1 state is very low, on the order of 150 ohms. This results in a high capacitive drive capability and consequently a fast rise time.

Wired logic functions are not allowed with this type of output. If wired logic is required, it may be desirable to use the IJ13. The IJ14 also has an identical logic configuration, but combines a DTL input with an "active pull-up" output.

However, when inputs of several gates are paralleled, their outputs may also be connected, in order to create one driver with greater fan-out than is available from a single power NAND. In this case the connection of several outputs to a single common point is legitimate because with the inputs connected in parallel all gates are at all times in the same state. Therefore, all outputs will also be at all times in the same state, and the dissipation rating of the output transistors on the IC chips will not be exceeded To obtain total fan-out capability in unit loads, multiply the number of parallel gates by 25.

The IJ64 is useful for driving ribbon cable because of the low output impedance.

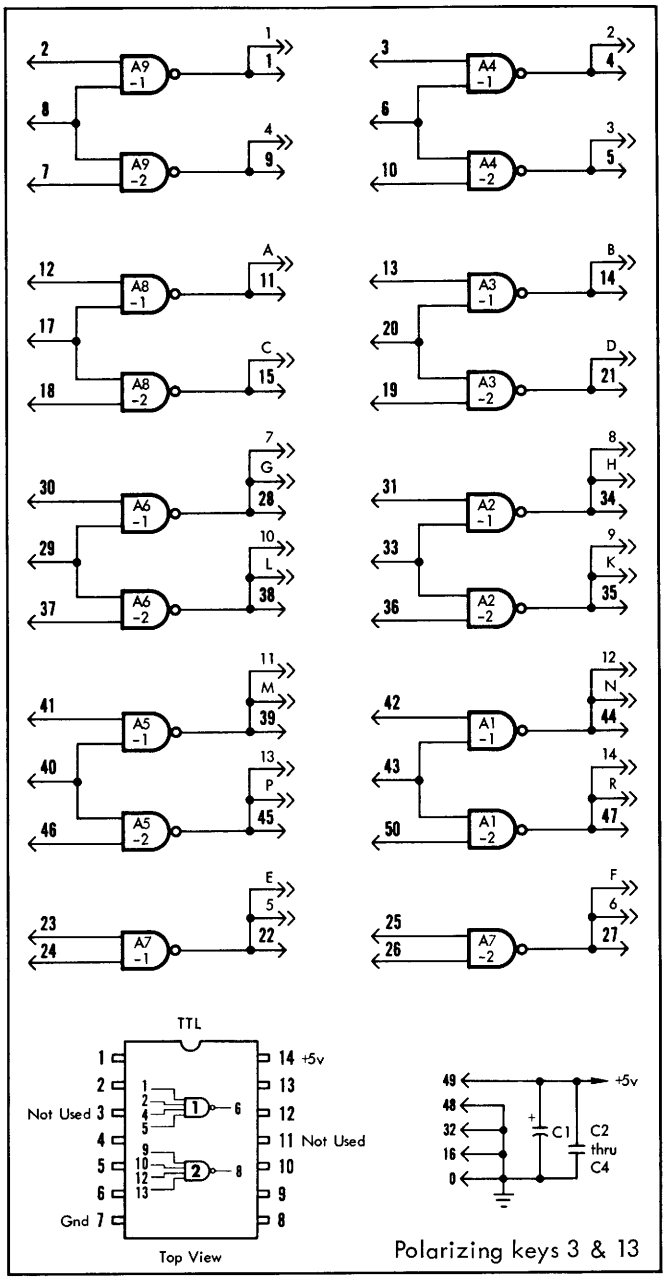
SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			25
Input loading	unit loads	all inputs			2
Propagation delay at 25°C, with load of 15 pf	ns			15	19
+5 volt supply (Vcc)	ma			108	596
Dissipation, per module	mw			540	3270

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 9	IC, power gate	9009	9
C1	Cap. tantalum, 1μf		1
C2, 3, 4	Cap. mylar, .01μf		3

LOGIC DIAGRAM



IJ66
4-INPUT POWER NANDS

The IJ66 module contains six power NANDs arranged in pairs with a strobe input common to each pair. Four independent power NANDs are also provided. The power gates used have multiple-emitter inputs and "active pull-up" outputs as is usually the case with TTL circuits.

The output impedance in the logic 1 state is very low, on the order of 150 ohms. This results in a high capacitive drive capability and consequently a fast rise time.

Wired logic functions are not allowed with this type of output. If wired logic is required, it may be desirable to use the IJ15. The IJ16 also has an identical logic configuration, but combines a DTL input with an "active pull-up" output.

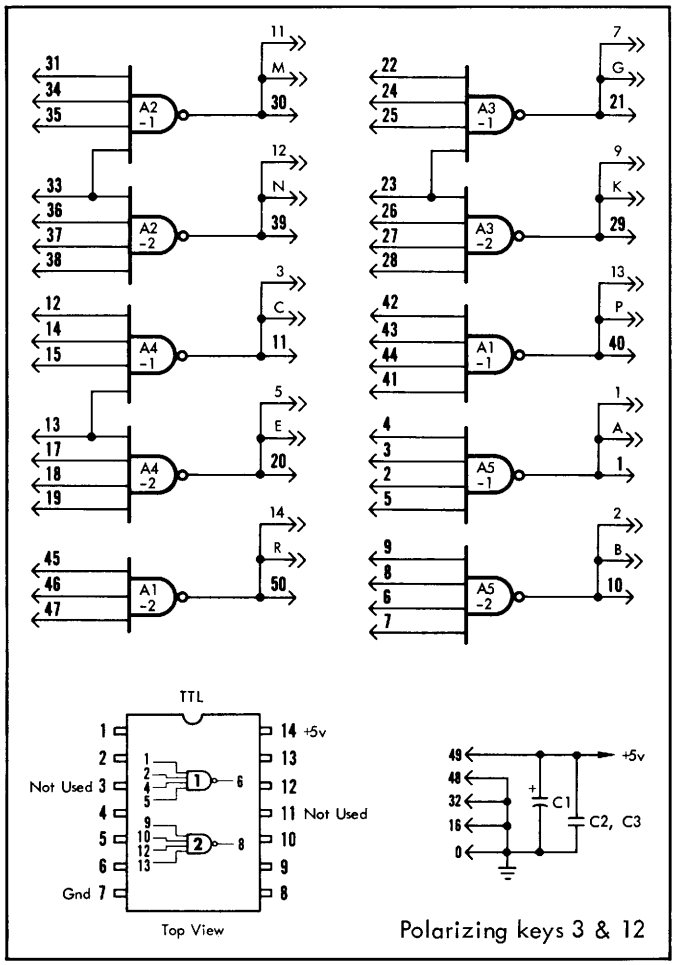
However, when inputs of several gates are paralleled, their outputs may also be connected, in order to create one driver with greater fan-out than is available from a single power NAND. In this case the connection of several outputs to a single common point is legitimate because with the inputs connected in parallel all gates are at all times in the same state. Therefore all outputs will also be at all times in the same state, and the dissipation rating of the output transistors on the IC chips will not be exceeded. To obtain total fan-out capability in unit loads, multiply the number of parallel gates by 25.

The IJ66 is useful for driving ribbon cable because of the low output impedance.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			25
Input loading	unit loads	all inputs			2
Propagation delay, at 25°C, with loads of 15pf	ns			15	19
+5 volt supply (Vcc)	ma			60	330
Dissipation, per module	mw			300	1815

LOGIC DIAGRAM



PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 5	IC, power gate	9009	5
C1	Cap. tantalum, 1μf		1
C2, 3	Cap. mylar, .01μf		2

LJ11
TRANSFER GATE (MULTIPLEXER) (DTL)

The LJ11 module is capable of transferring (multiplexing) one of four groups, each having eight signals, onto a single group of eight lines. The transfer is accomplished using NAND gates; therefore, the information on the output lines is the inverse of that on the input lines. A low signal (logic 0) is used to transfer or strobe each of the four groups of eight signals onto the eight output lines whenever desired. This is usually done one at a time. The inversion symbol (small circle) is placed at the input of each strobe inverter to indicate that logic 0 (low) is required to cause a transfer.

Note that the common connections of NANDs on the output lines form wired AND functions. The combination of an AND preceded by four inverters forms a NOR:

$$Q = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} = \overline{A + B + C + D}.$$

Therefore, the module can be used as eight independent 4-input NORs by holding all four strobe inputs low simultaneously.

SPECIFICATIONS

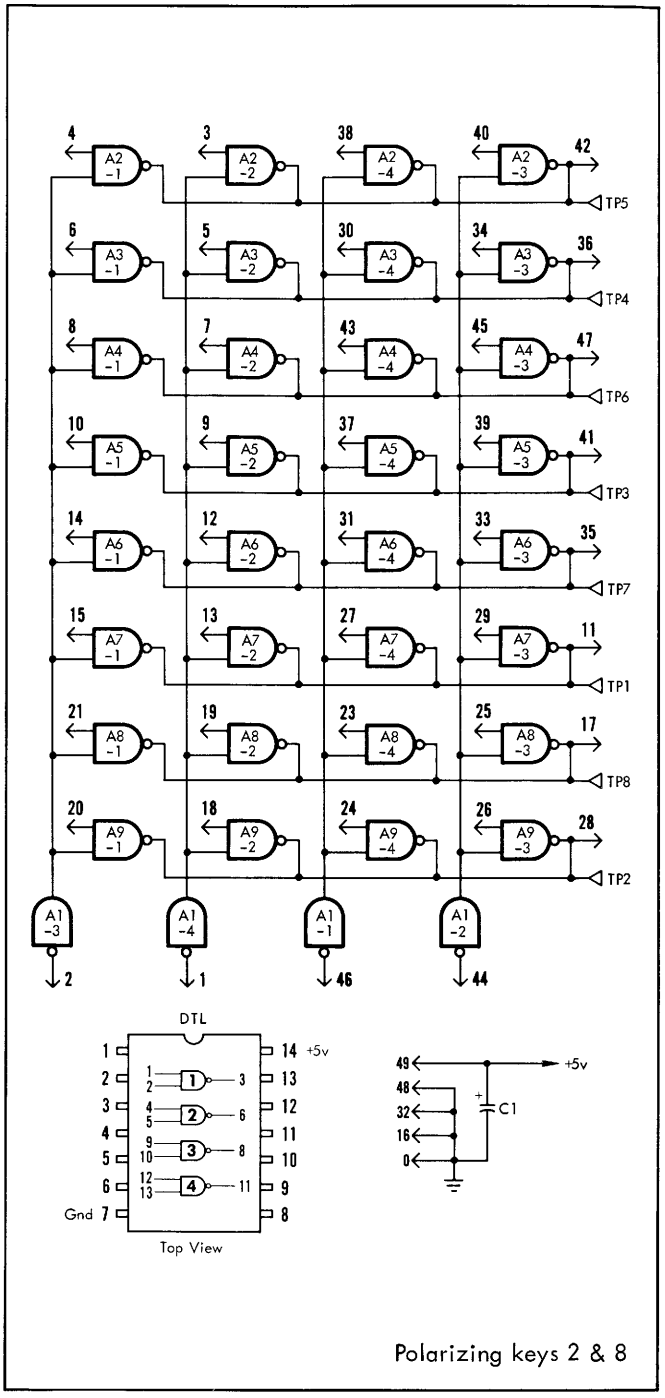
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	all outputs			5-1/2
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf (from strobe leading edge)	ns			55	88
+5 volt supply (Vcc)	ma			63	90*
Dissipation, per module	mw			288	444*

*at +5.5v

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 9	IC gate, quad 2-in	946	9
C1	Cap., mylar, .01μf		1

LOGIC DIAGRAM



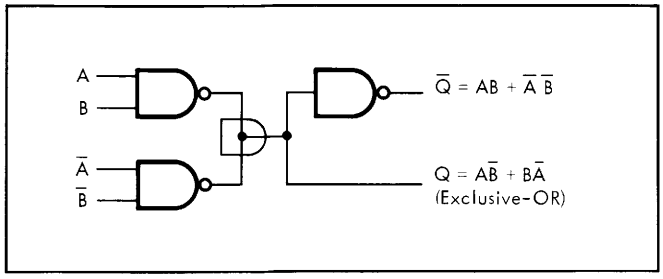
Polarizing keys 2 & 8

The LJ12 contains seven AND/NOR gates with complementary outputs, and one logic driver/inverter. Each gate performs both functions $Q = AB + CD$ and $\overline{Q} = \overline{AB + CD}$. If used for the Exclusive-OR function, apply complementary inputs of the same two signals as shown in the example.

The logic driver/inverter consists of three inverters connected so that the outputs of two inverters are additive (because inputs are connected as well as outputs), causing the unit to operate as a high-fanout driver. The third inverter, A4-3, is used at the driver input to allow optional inversion.

EX-ORs are extremely useful for constructing adders, comparators, and parity generators. Outputs may be connected together to form wired logic functions in this DTL version.

The LJ12 uses DTL circuits. For a TTL version refer to LJ62.



Example Of Gate Used As Exclusive-OR

SPECIFICATIONS

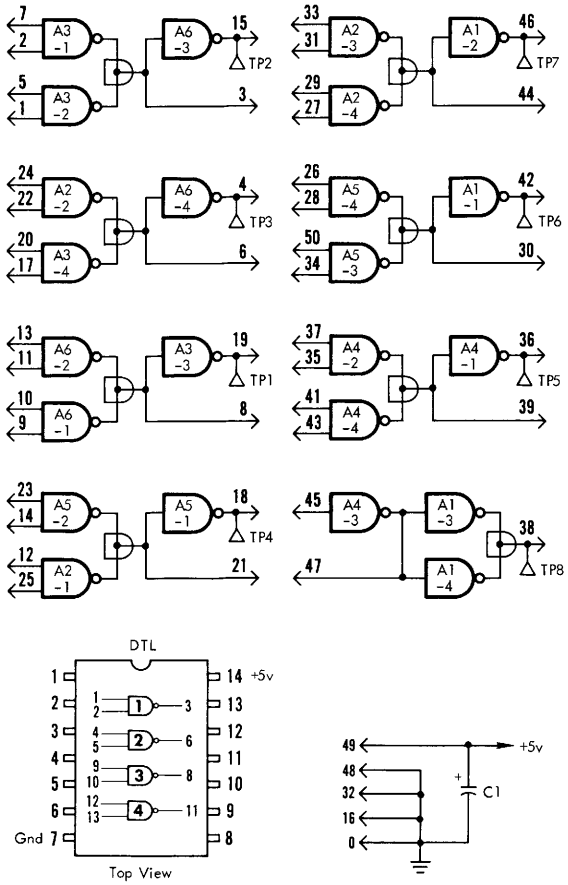
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL	unit loads	15, 4, 19, 18, 46, 42, 36 3, 6, 8, 21, 44, 30, 39 38			8 6 16
Input loading	unit loads	47 All others			3 1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf (through 2 inverters) Propagation delay (through 1 inverter)	ns			55 31	88 51
+5 volt supply (Vcc)	ma			43	60.4*
Dissipation, per module	mw			215	332*

*at +5.5v

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 6	IC gate, quad 2-in	946	6
C1	Cap., mylar, .01μf		1

LOGIC DIAGRAM



Polarizing keys 2 & 17

LJ16
4-BIT PARALLEL BINARY ADDER (DTL)

The LJ16 module contains a 4-bit parallel binary full-adder with ripple carry between stages. The module also contains four 2-input NANDs which permit the adder to be used with single-ended (True input only) data signals. The NANDs can be used for other logic functions if not needed at adder input. Refer to logic diagrams 1 and 2, and schematic diagram.

Two or more LJ16 modules can be cascaded to increase the number of adder stages. This expansion is limited only by the allowable increase in delay through the adder due to the ripple carry propagation. With an external Carry Flip-flop one parallel adder can be used in a serial-parallel fashion to extend its range. In this mode, addition takes place n-bits at a time in parallel, with any number of n-bit groups added serially, using one add time per add cycle. (One add time is the propagation delay through the entire 4-bit circuit).

With an external storage register the adder can be used to create an accumulator. (An accumulator stores a number which can be made either larger or smaller). The adder generates both True and False outputs of the Sum digits.

The adder can also be used to add less than four bits in parallel because all of the Carry outputs are available.

The module is used as a subtractor by inputting the 1's complement of one of the two 4-bit characters to be added, also adding a 1 to the least significant bit (LSB), and ignoring the MSB carry out, if present. The 1's complement is generated by inverting each bit in the character. For example, the 1's complement of 1001 is 0110. Thus to subtract 1001 from 1111, add 0110 to 1111, place a 1 into the LSB Carry input, and ignore the MSB Carry out.

```
    1111
    0110
       1
   -------
ignore --- 1 | 0110 --- difference
```

Note that when the signals are connected as shown in logic diagrams 3 and 4, the adder provides the function of complementing Y inputs. The carry-in, C1, is also complemented, which is equivalent to adding a 1 to the LSB. Compare logic diagrams 3 and 1, or 4 and 2.

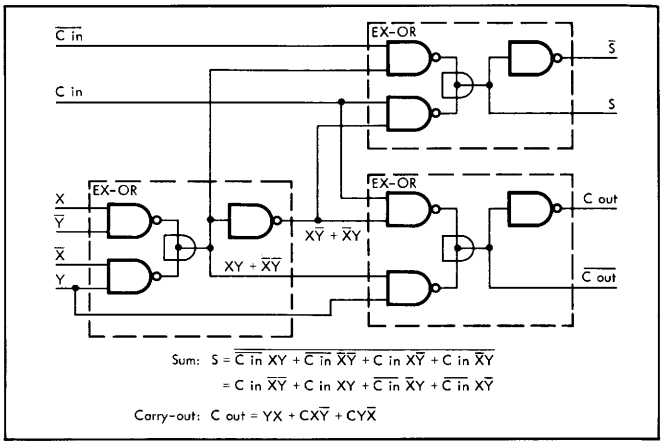
To use the module as a 4-bit comparator, connect as a subtractor. When the two inputs are equal the sum is zero. When Y is smaller than X the carry-out is 1. When Y is greater than X the carry-out (C5) is zero.

PARTS LIST

Designator	Description	Type	Qty.
A1 thru 10	IC gate, quad 2-in	946	10
C1	Cap., mylar .01μf		1

Each 1-bit portion of the adder is made up of three exclusive OR circuits connected together as a full adder, similar to the circuit shown below. Note, however, that the four adder circuits are not identical (see schematic, page 92). The arrangement that is used reduces carry propagation time.

The LJ16 uses DTL circuits. For a TTL version see LJ66.



SPECIFICATIONS

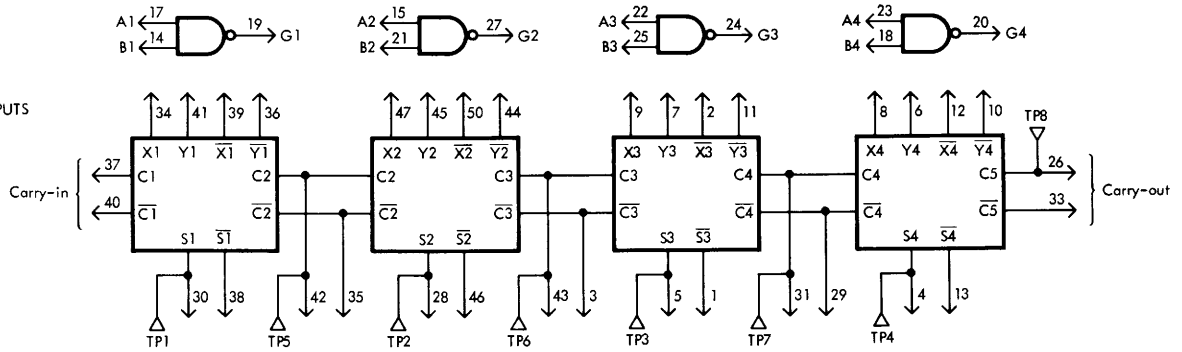
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL (Addition mode) S outputs S outputs C2, C3, C4 C2, C3, C4 C5 C5 Independent Gates	unit loads 	 30, 28, 5, 4 38, 46, 1, 13 42, 3, 31 35, 43, 29 26 33 19, 27, 24, 20			 6 8 7 4 6 8 8
Input loading (Addition mode) C1 input C1, C2, C3, C4 C2, C3, C4 X1, X1, X2, X3, X3, X4 X2, X4 Y1, Y2, Y2, Y3, Y4, Y4 Y1, Y3 A, B	unit loads 	 40 37, 42, 3, 31 35, 43, 29 34, 39, 47, 9, 2, 8 50, 12 36, 45, 44, 11, 10, 6 41, 7 17, 14, 15, 21, 22, 25, 23, 18			 1 2 4 1 2 1 2 1
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf (through 3 NANDs) (through 4 NANDs) (through entire adder)	ns			112.7 143.7 241.5	200 252 314
+5 volt supply (Vcc)	ma			72	101*
Dissipation, per module	mw			360	555*

*at +5.5v

LOGIC DIAGRAM, LJ16

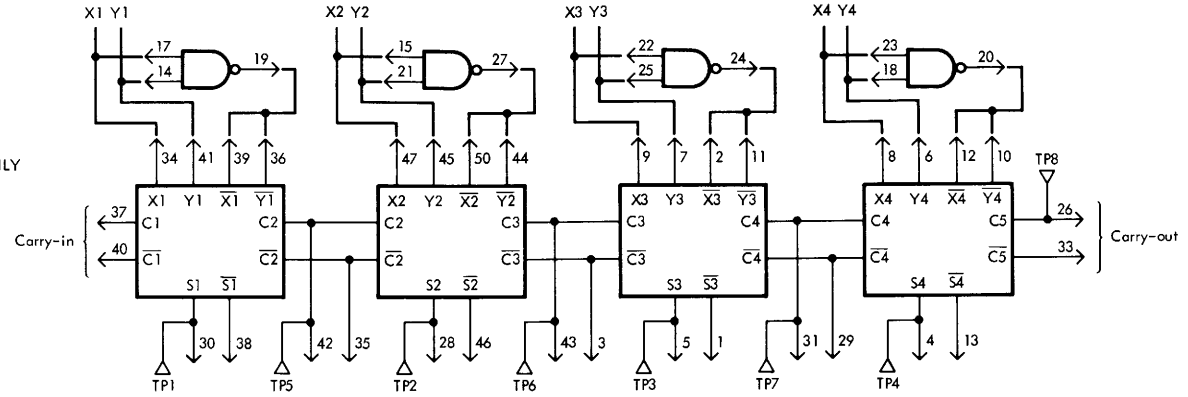
1. Connections on Adder for Addition, Using Both True and False Inputs

S = X PLUS Y,
TRUE AND FALSE INPUTS



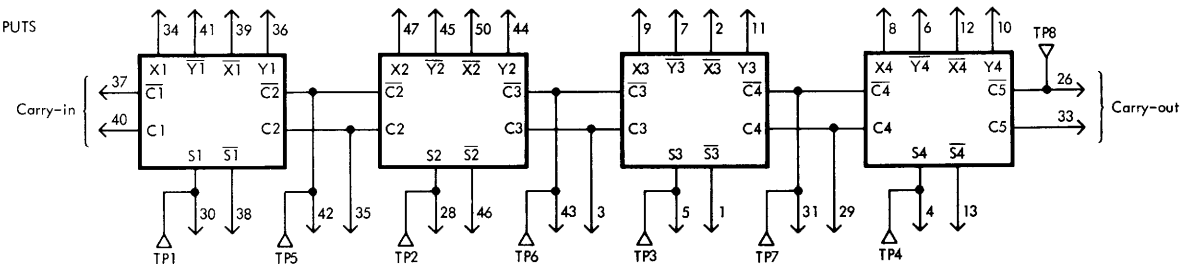
2. Connections on Adder for Addition, Using Only True Inputs

S = X PLUS Y,
TRUE INPUTS ONLY



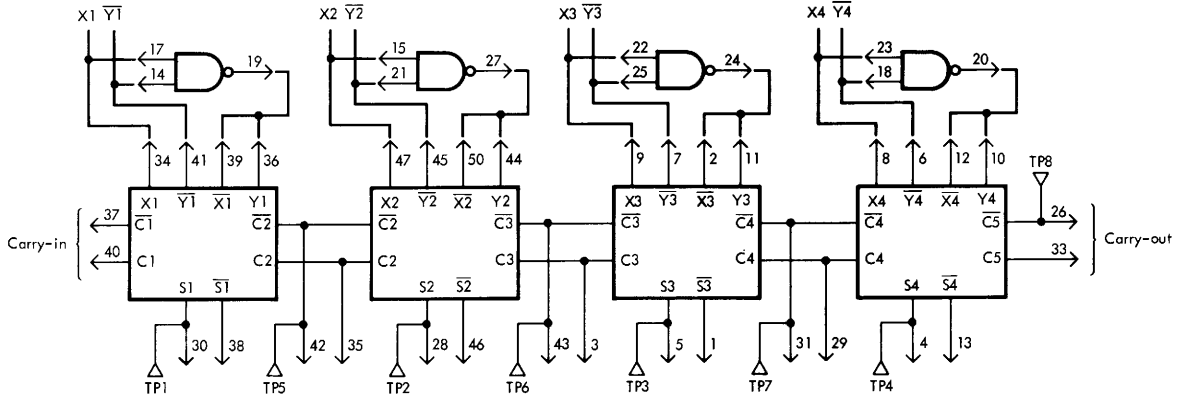
3. Connections on Adder for Subtraction, Using Both True and False Inputs

S = X - Y,
TRUE AND FALSE INPUTS



4. Connections on Adder for Subtraction, Only One Logic Phase at Inputs

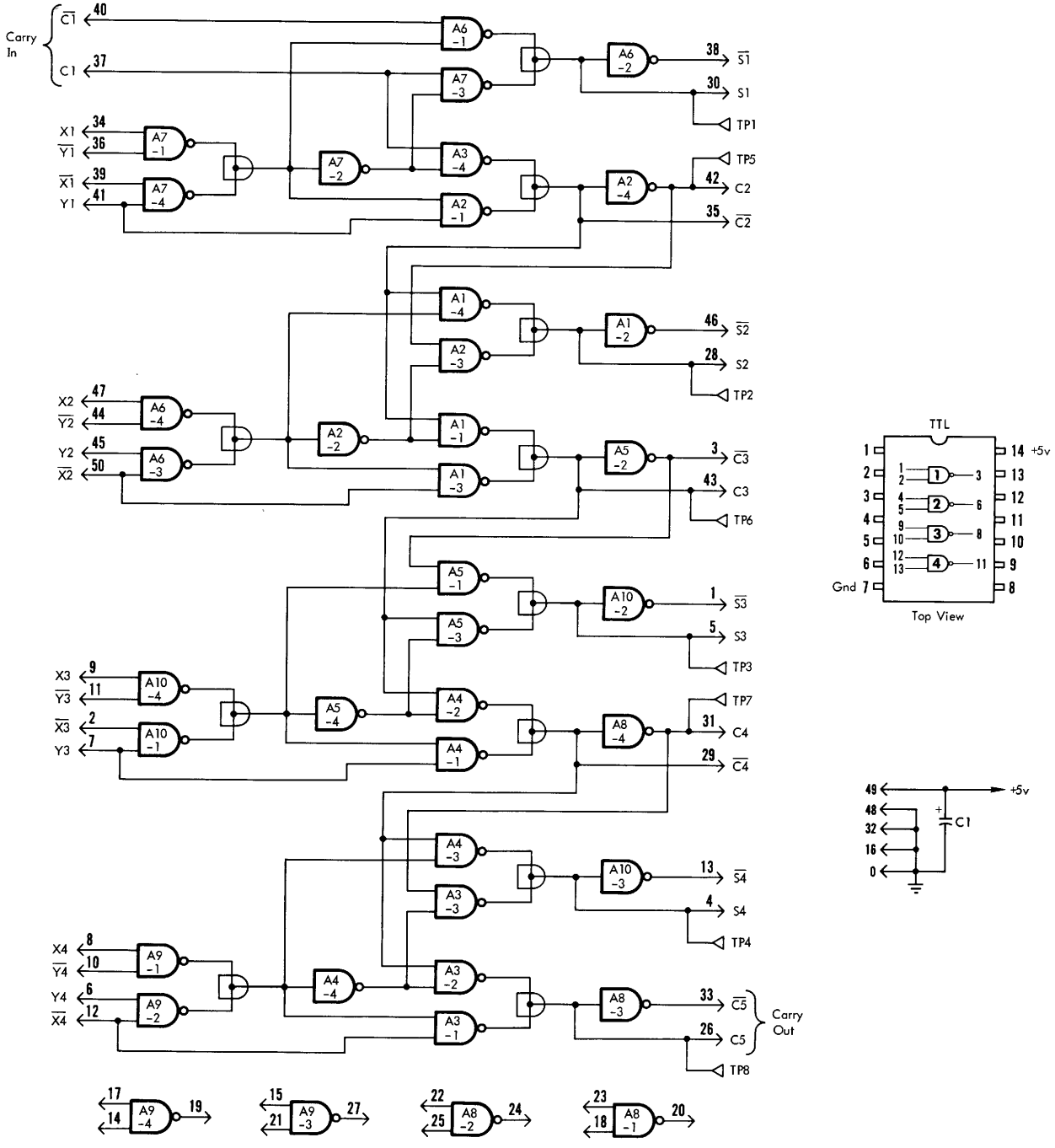
S = X - Y



Note: S = sum. X and Y are the bits to be added. C1 is carry-in. C2 is carry-out of first stage and carry-in to second stage. C3 is carry-out of second stage and carry-in to third stage. C4 is carry-out of third stage, and carry-in to fourth stage. C5 is carry-out of adder. A and B are independent NAND gate inputs, and G is NAND gate output (see schematic diagram on next page).

SCHEMATIC DIAGRAM, LJ16

Polarizing keys 2 & 15



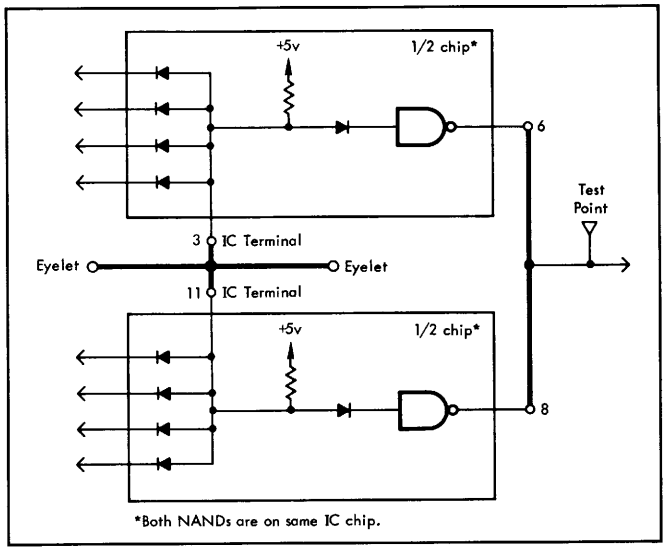
NOTE: Logic notation shown is for addition, using both True and False inputs.

LJ17 contains five 8-input NANDs, each composed of two 4-input NANDs on a single type 930 chip, connected via etch as shown below. Because both inputs and outputs of the two inverters are paralleled, input loading and fan-out are doubled.

To expand fan-in, jumper eyelets on the board (not at the backplane) as given below. Outputs may also be connected together, at the backplane, if desired.

To Form	Jumper eyelets
16-input gate	E1-E2 or E3-E4 or E5-E6 or E7-E8
24-input gate	any neighboring two pair above, such as E1-E2-E3-E4
32-input gate	any neighboring three pair above
40-input gate	all four pair

Wired logic functions can also be created at the outputs by connecting only outputs together, leaving eyelets disconnected.

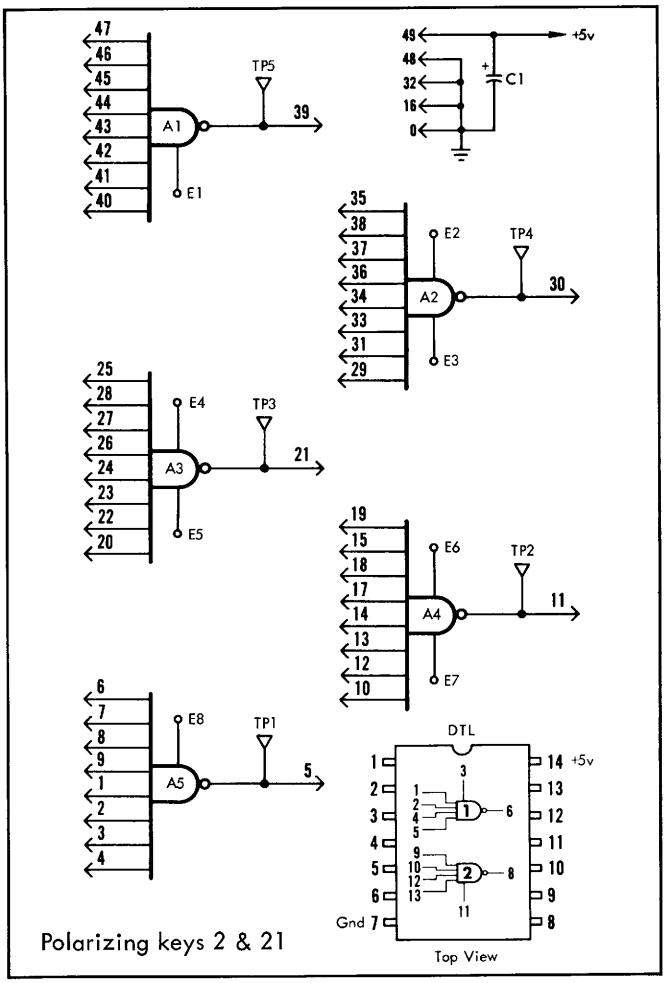


SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into DTL Each output	unit loads	39, 30, 21, 11, 5			16
(when eyelets and outputs are connected to expand the fan-in, add fan-outs. For example, a 16-input gate has a fan-out of 32.)					
Input loading	unit loads				2
(per input, when no eyelets are jumpered. If eyelets are connected, input loading increases by 2 unit loads per input for each expansion. For example, a 16-input gate exhibits a loading of 4 unit loads per input; a 32-input gate exhibits a loading of 8 unit loads per input.)					
Propagation delay, at 25°C, with loads of 12.8 ma/30 pf	ns			31	51
+5 volt supply (Vcc)	ma			18	25.2*
Dissipation, per module	mw			90	138.5*

* at +5.5v

LOGIC DIAGRAM



PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 5	IC gate, dual 4-in	930	5
C1	Cap., mylar .01μf		1

LJ61
TRANSFER GATE (MULTIPLEXER) (TTL)

The LJ61 module is capable of transferring (multiplexing) one of four groups, each having eight signals, onto a single group of eight lines. The transfer is accomplished using AND/NOR gates; therefore, the information on the output lines is the inverse of that on the input lines. A low signal (logic 0) is used to transfer or strobe each of the four groups of eight signals onto the eight output lines whenever desired. This must be done one at a time. The inversion symbol (small circle) is placed at the input of each strobe inverter to indicate that logic 0 (low) is required to cause a transfer.

The outputs of the NOR circuits may not be wired together.

The LJ61 uses TTL circuits. For a DTL version see LJ11.

SPECIFICATIONS

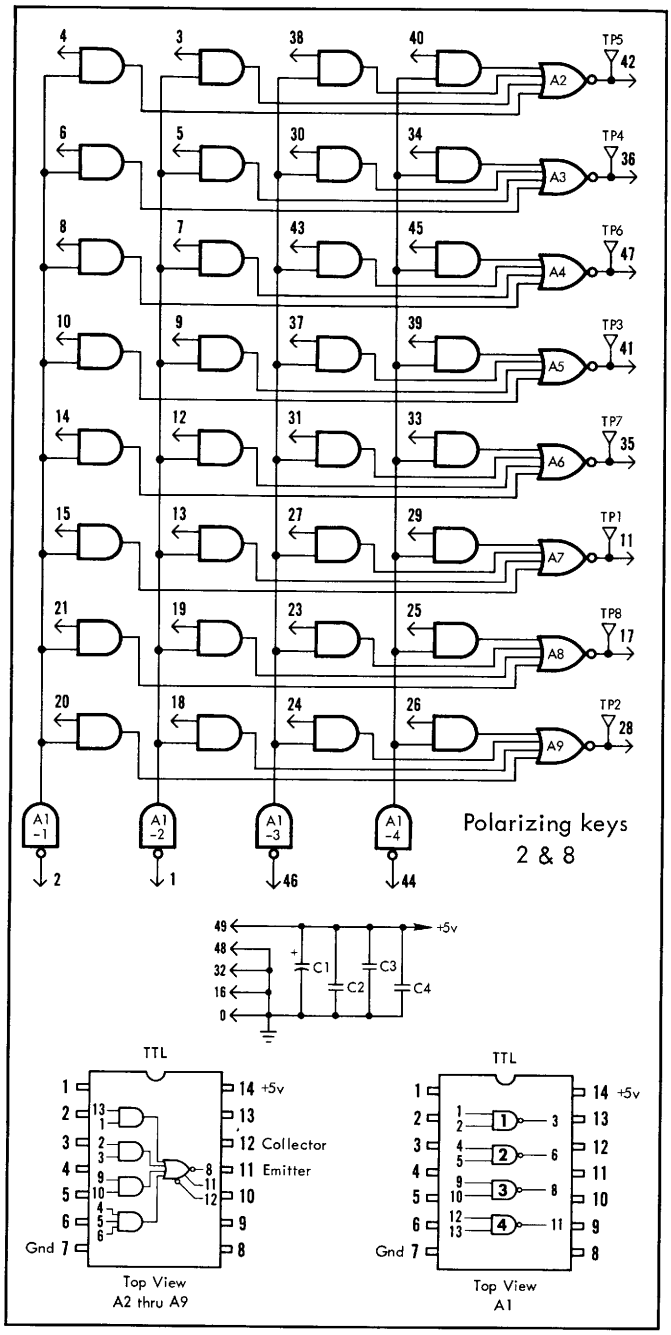
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	all outputs			8
Input loading	unit loads	all inputs			1
Propagation delay, at 25°C, with loads of 15 pf (after strobe leading edge)	ns			25	33
+5 volt supply (Vcc)	ma			64.8	396*
Dissipation, per module	mw			324	2, 180*

* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 9	IC gate, quad 2-in	9002	9
C1	Cap., tantalum, 1μf		1
C2, 3, 4	Cap., mylar, .01μf		3

LOGIC DIAGRAM

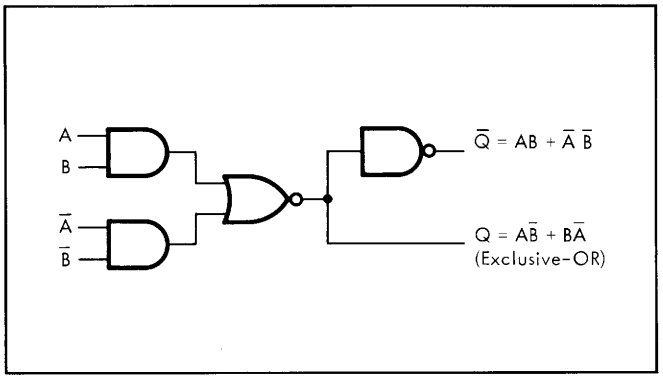


The LJ62 contains seven AND-NOR gates with complementary outputs, and one logic driver/inverter. Each gate performs both functions $Q = AB + CD$ and $\overline{Q} = \overline{AB + CD}$. If used for the Exclusive-Or function, apply complementary inputs of the same two signals as shown in the example.

The logic driver/inverter consists of three circuits connected so that the outputs of two NANDs are additive (because inputs are connected as well as outputs), causing the unit to operate as a high-fanout driver. The inverter A1-1 is used at the driver input to allow optional inversion.

EX-ORs are extremely useful for constructing adders, comparators, and parity generators. However, outputs cannot be connected together to form wired logic functions in this TTL version.

For a DTL version see LJ12.



Example Of Gate Used As Exclusive-OR

SPECIFICATIONS

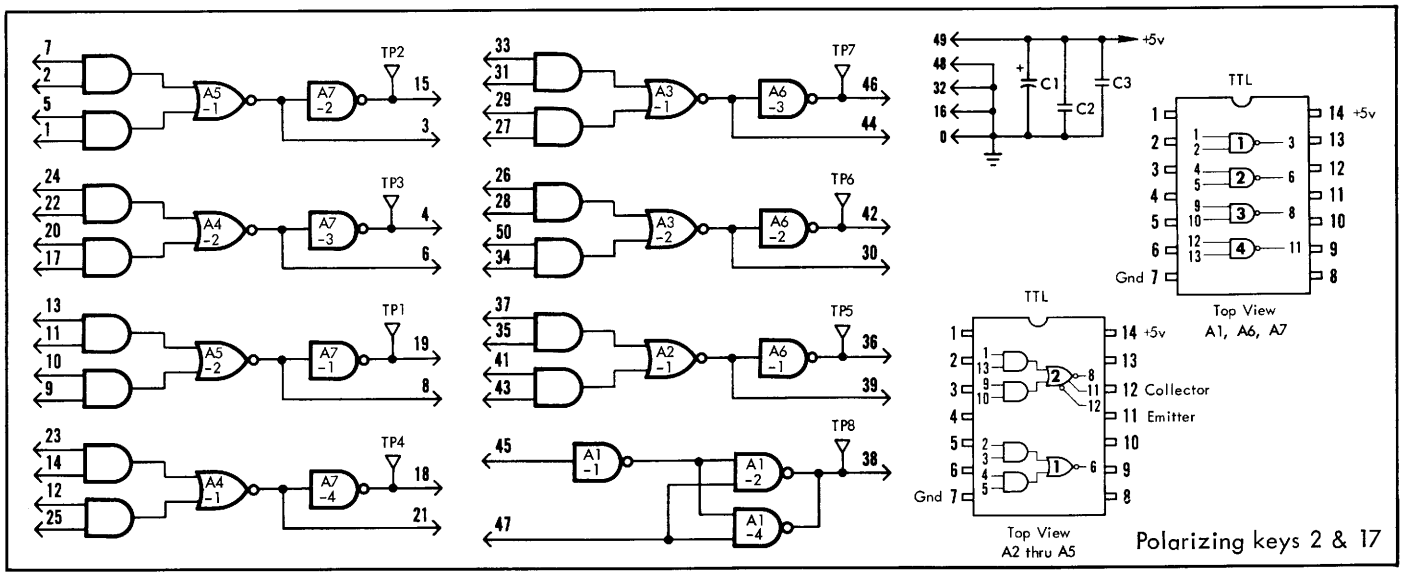
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level Logic 0 level	volts volts		2.4 0		5.5 0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads	15, 4, 19, 18, 46, 42, 36 3, 6, 8, 21, 44, 30, 39 38			8 7 16
Input loading	unit loads	47 All others			2 1
Propagation delay, at 25°C, with loads of 15 pf	ns			25	33
+5 volt supply (Vcc)	ma			38	232.4*
Dissipation, per module	mw			190	1278.2*

* at +5.5v and 20 MHz

PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 6	IC gate, quad 2-in	9002	6
C1	Cap., tantalum, 1μf		1
C2, 3, 4	Cap., mylar, .01μf		3

LOGIC DIAGRAM



LJ66
4-BIT PARALLEL BINARY ADDER (TTL)

The LJ66 module contains a 4-bit parallel binary full-adder with ripple carry between stages. The module also contains four 2-input NANDs which permit the adder to be used with single-ended (True input only) data signals. The NANDs can be used for other logic functions if not needed at adder input. Refer to logic diagrams 1 and 2, and schematic diagram.

Two or more LJ66 modules can be cascaded to increase the number of adder stages. This expansion is limited only by the allowable increase in delay through the adder due to the ripple carry propagation. With an external Carry Flip-flop one parallel adder can be used in a serial-parallel fashion to extend its range. In this mode, addition takes place n-bits at a time in parallel, with any number of n-bit groups added serially, using one add time per add cycle. (One add time is the propagation delay through the entire 4-bit circuit).

With an external storage register the adder can be used to create an accumulator. (An accumulator stores a number which can be made either larger or smaller). The adder generates both True and False outputs of the Sum digits.

The adder can also be used to add less than four bits in parallel because all of the Carry outputs are available.

The module is used as a subtractor by inputting the 1's complement of one of the two 4-bit characters to be added, also adding a 1 to the least significant bit (LSB), and ignoring the MSB carry out, if present. The 1's complement is generated by inverting each bit in the character. For example, the 1's complement of 1001 is 0110. Thus to subtract 1001 from 1111, add 0110 to 1111, place a 1 into the LSB Carry input, and ignore the MSB Carry out.

```
      1111
      0110
         1
     -------
ignore  1 0110  difference
```

Note that when the signals are connected as shown in logic diagrams 3 and 4, the adder provides the function of complementing Y inputs. The carry-in, C1, is also complemented, which is equivalent to adding a 1 to the LSB. Compare logic diagrams 3 and 1, or 4 and 2.

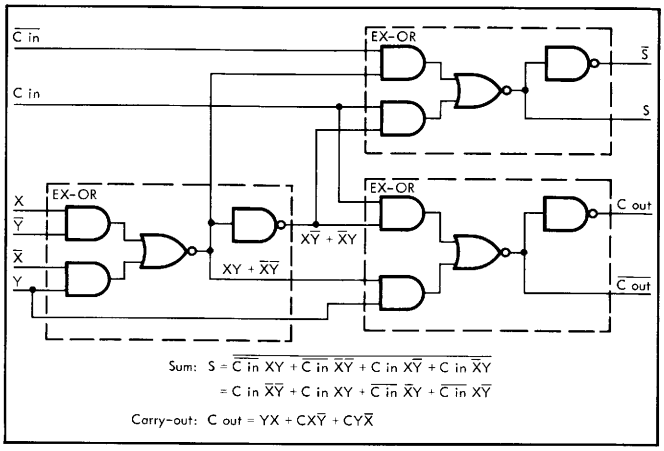
To use the module as a 4-bit comparator, connect as a subtractor. When the two inputs are equal the sum is zero. When Y is smaller than X the carry-out is 1. When Y is greater than X the carry-out (C5) is zero.

PARTS LIST

Designator	Description	Type	Qty.
A1 thru 10	IC gate, quad 2-in	9002	10
C1	Cap., tantalum, 1μf		1
C2, 3, 4	Cap., mylar, .01μf		3

Each 1-bit portion of the adder is made up of three exclusive OR circuits connected together as a full adder, similar to the circuit shown below. Note, however, that the four adder circuits are not identical (see schematic, page 98). The arrangement that is used reduces carry propagation time.

The LJ66 uses TTL circuits. For a DTL version see LJ16.



SPECIFICATIONS

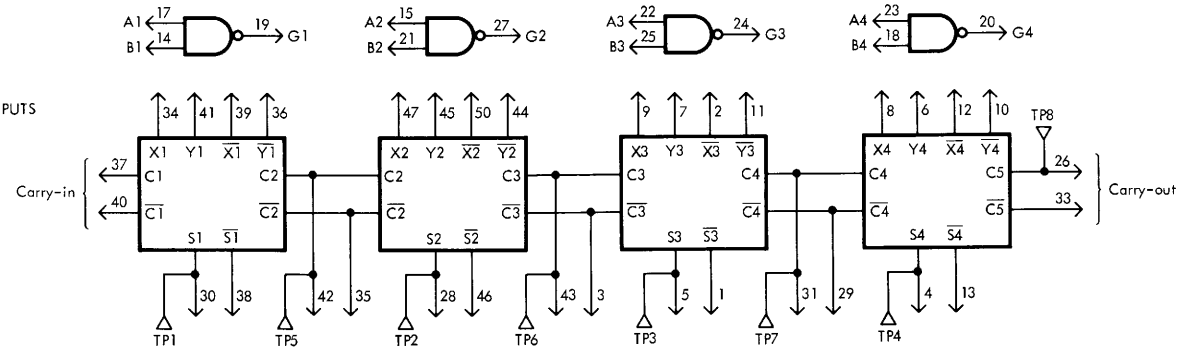
Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		20
Logic 1 level	volts		2.4		5.5
Logic 0 level	volts		0		0.4
Switching threshold	volts			1.5	
Fan-out, into TTL	unit loads				
S outputs		30, 28, 5, 4			7
$\overline{S}$ outputs		38, 46, 1, 13			8
$\overline{C2}$, $\overline{C3}$, $\overline{C4}$		35, 43, 29			5
C2, $\overline{C3}$, C4, C5		42, 3, 31, 26			7
$\overline{C5}$		33			8
G outputs		19, 27, 24, 20			8
Input loading (Addition mode)	unit loads				
C1 input		37			2
$\overline{C1}$ input		40			1
X1, $\overline{X1}$, X2, X3, $\overline{X3}$, X4		34, 39, 47, 9, 2, 8			1
$\overline{X2}$, $\overline{X4}$		50, 12			2
$\overline{Y1}$, Y2, $\overline{Y2}$, $\overline{Y3}$, Y4, $\overline{Y4}$		36, 45, 44, 11, 6, 10			1
Y1, Y3		41, 7			2
A, B		17, 14, 15, 21, 22, 25, 23, 18			1
Propagation delay, at 25°C, with loads of 15 pf	ns				
(through 3 stages--i.e., S outputs)				40	52
(through 4 stages--i.e., $\overline{S}$ outputs)				50	66
(through entire adder)				85	109
+5 volt supply (Vcc)	ma			56.8	259.6*
Dissipation, per module	mw			284	1427.8*

* at +5.5v and 20 MHz

LOGIC DIAGRAM, LJ66

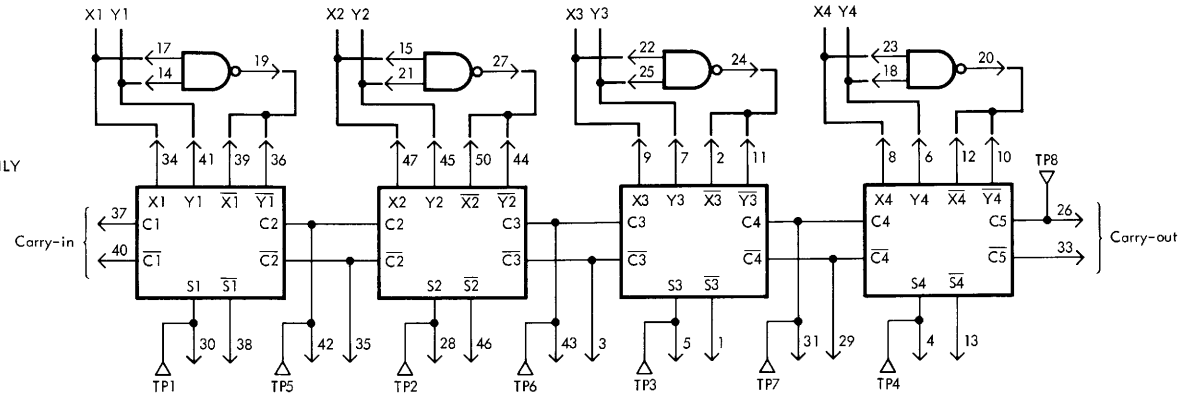
1. Connections on Adder for Addition, Using Both True and False Inputs

S = X PLUS Y,
TRUE AND FALSE INPUTS



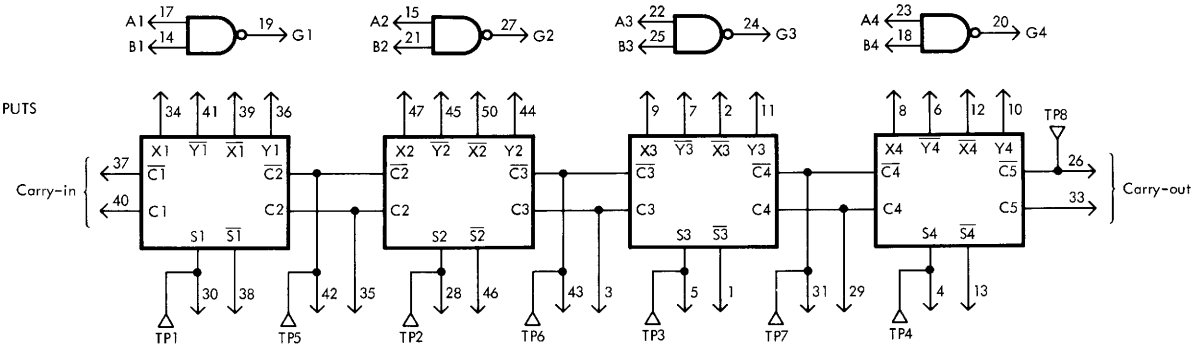
2. Connections on Adder for Addition, Using Only True Inputs

S = X PLUS Y,
TRUE INPUTS ONLY



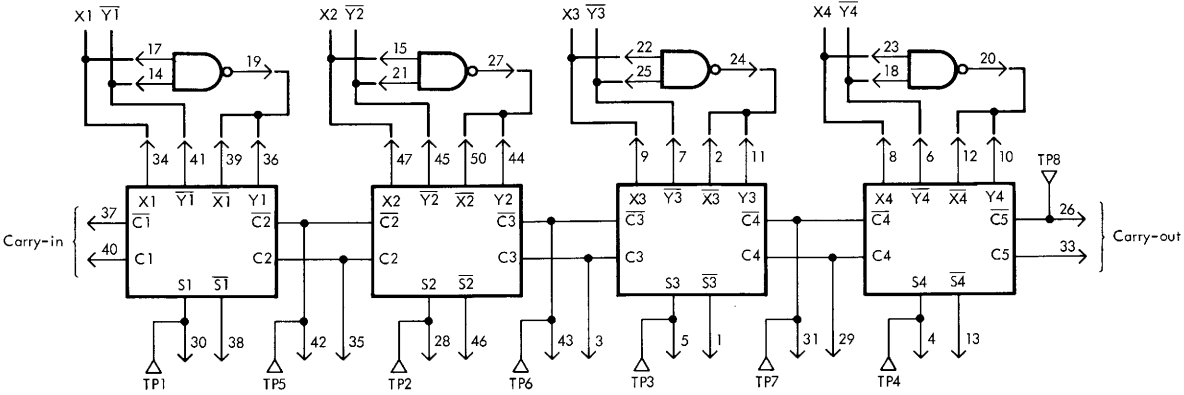
3. Connections on Adder for Subtraction, Using Both True and False Inputs

S = X − Y,
TRUE AND FALSE INPUTS



4. Connections on Adder for Subtraction, Only One Logic Phase at Inputs

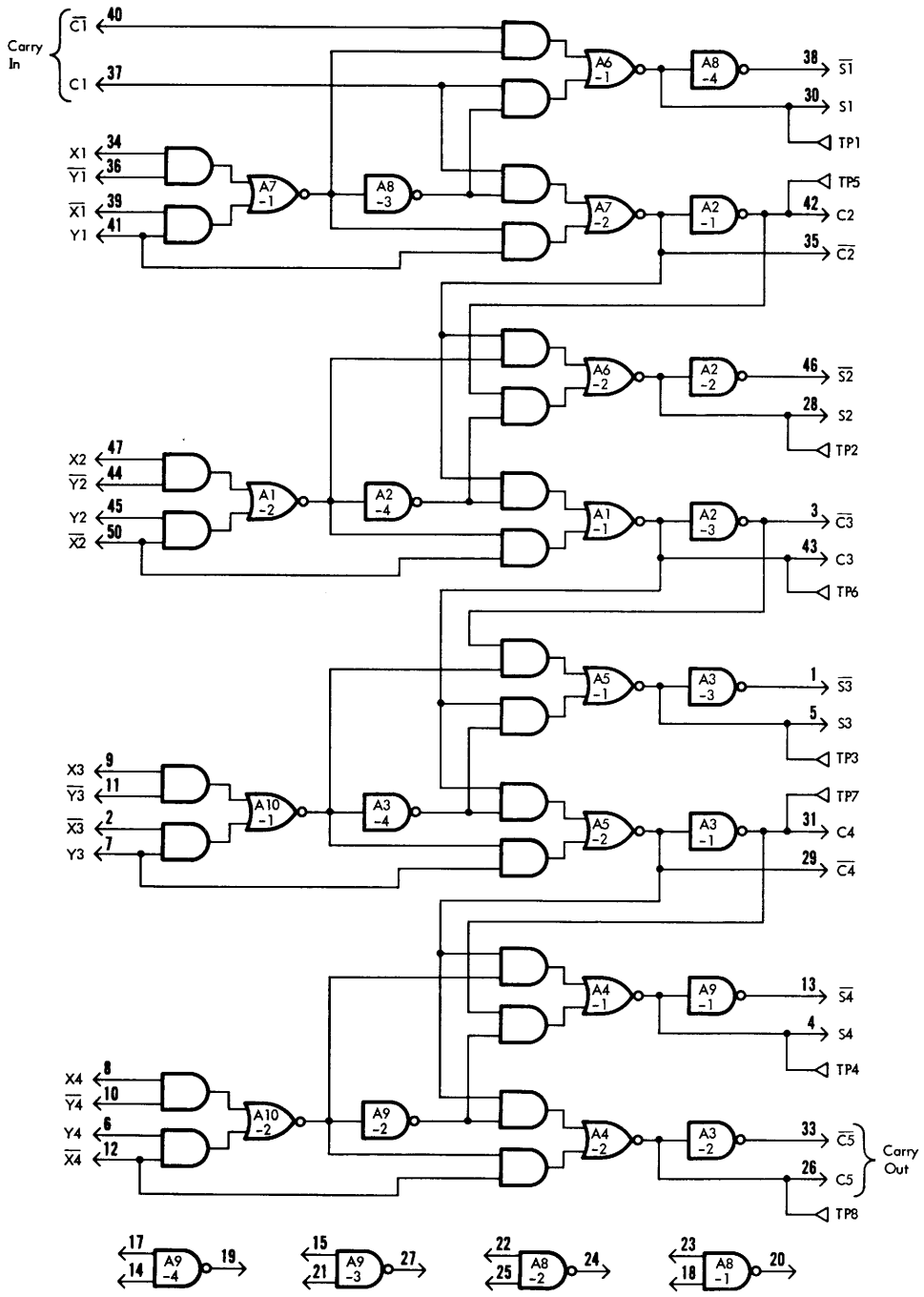
S = X − Y

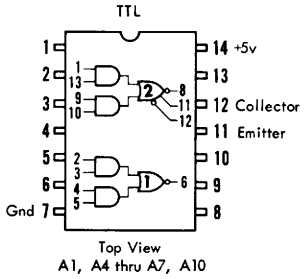


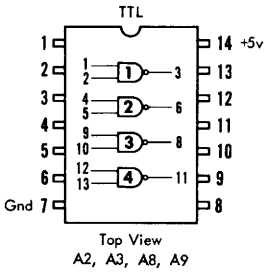
Note: S = sum. X and Y are the bits to be added. C1 is carry-in. C2 is carry-out of first stage and carry-in to second stage. C3 is carry-out of second stage and carry-in to third stage. C4 is carry-out of third stage, and carry-in to fourth stage. C5 is carry-out of adder. A and B are independent NAND gate inputs, and G is NAND gate output (see schematic diagram on next page).

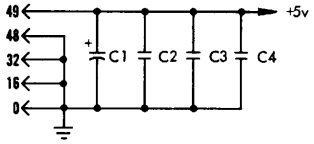
SCHEMATIC DIAGRAM, LJ66

Polarizing keys 2 & 15









NOTE: Logic notation shown is for addition, using both True and False inputs.

NT18
NEGATIVE-LOGIC TO SDS INTERFACE

The NT18 module contains eight discrete component 2-input gates which accept 0v and -v input logic levels and convert to standard J Series output logic levels. When both inputs are low (-v) the output becomes high (+5v). When either or both inputs are high (0v) the output becomes low (0v). A negative voltage as low as -25 volts can be used as input low logic level.

Either of two switching thresholds can be used at the input, as determined by the presence or absence of a jumper wire on each gate. When input logic level exceeds -6v, use the -4.6v switching threshold (no jumper). When input logic level does not exceed -6v use the -2.4v switching threshold (use jumper).

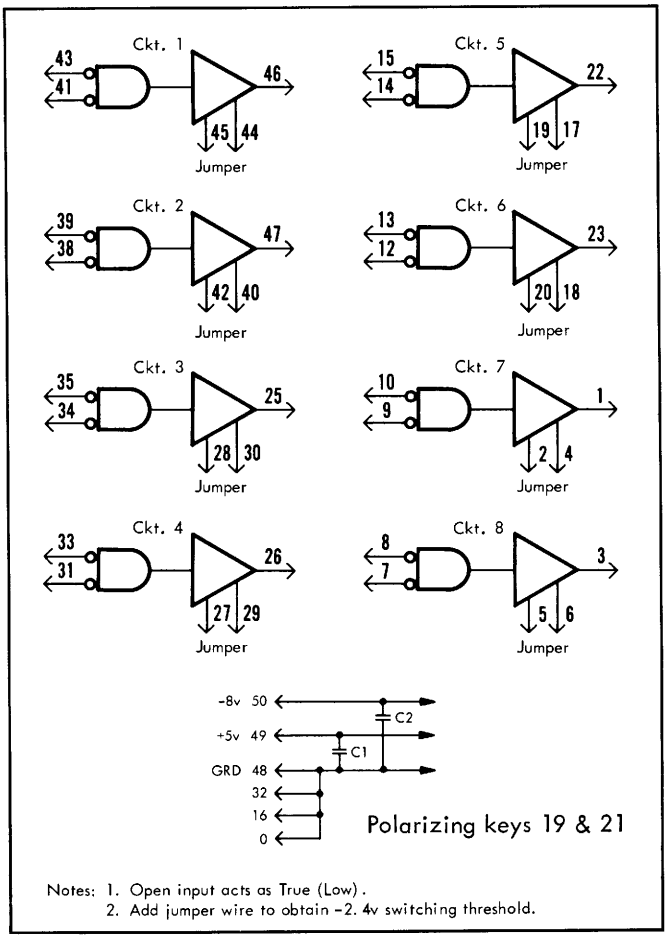
Refer to NT18 data sheet for schematic and parts list, and for instructions which describe how to vary the switching threshold.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Data rate	MHz		0		2
Inputs					
Logic low level	volts		-3.4*		-25
Logic high level	volts		0		-0.4
Input loading	ma	see diagram		4	
Switching threshold					
with jumper	volts			-2.4	
without jumper	volts			-4.6	
Outputs					
Logic 1 level	volts		4.5		5.5
Logic 0 level	volts		0		0.4
Fan-out, into DTL	unit loads	see diagram			33
Fan-out, into TTL	unit loads				27
Propagation delay, at 25°C	ns			40	100
+5 volt supply (Vcc)	ma			144	156
-8 volt supply	ma			65	100
Dissipation, per module	mw			1.24	1.58†

* -3.4v is recommended as the smallest -v, to maintain 1 volt noise rejection.
† At 10% over nominal supply voltages.

LOGIC DIAGRAM



Notes: 1. Open input acts as True (Low).
2. Add jumper wire to obtain -2.4v switching threshold.

Truth Table		
Input A	Input B	Output
0v	0v	0v
0v	-v	0v
-v	0v	0v
-v	-v	+5v

NT33
SDS TO NEGATIVE-LOGIC INTERFACE

The NT33 module contains eight 2-input gates which accept standard J Series logic levels as input and furnish 0v and -v logic levels as output. A negative voltage as low as -30 volts can be used as a negative logic level. It must be supplied from an external source and wired to pin 17.

When either or both inputs are low (0v) the output is high (0v). When both inputs are high (+5v) the output is low (-v).

Truth Table		
Input A	Input B	Output
0v	0v	0v
+5v	0v	0v
0v	+5v	0v
+5v	+5v	-v

The NT33 is similar to the previously sold NT17. The important differences between the two modules are:

1. The NT33 will accept -v down to -30 volts; the NT17 will accept -12 volts.
2. NT33 max. output sinking current is 140 ma over its output voltage range; max. NT17 current is 20 ma.
3. NT33 rise and fall times are controlled with a capacitor (C4).
4. NT33 provides a high output impedance to the line (>200K ohms) when power is off.

The NT33-1 module is a variation on the NT33 design. The NT33 shows a power-on output impedance of 2.35 Kohms, acceptable for a 0 to -15 volt interface application. The NT33-1 has an equivalent 150 ohm output resistance for cases where a closer match to cable or interface impedance is desired, as in low voltage (i.e. 0v to -3.0v) interfacing. In either case, twisted-pair or coaxial cabling is usually a good choice for distances up to 200 feet.

The NT33 provides an excellent match with Univac and CDC equipment, meeting all specifications.

The NT33 and NT33-1 drivers can be paired with either NT18 or AT69 receivers, depending on input noise level and logic swings. The AT69 differential receiver can tolerate higher cable noise than the NT18. The combination of NT33-1 with AT69 forms an excellent interface for Univac low logic level equipment.

Other variations to NT33 output impedance and rise/fall time can be made on special order.

For detailed schematic and parts list refer to NT33 data sheet.

SPECIFICATIONS

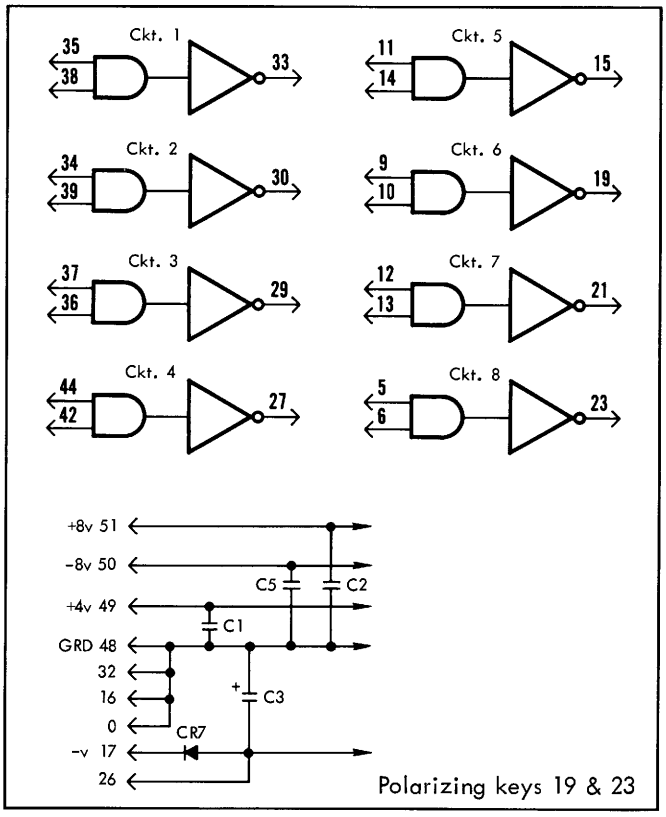
Characteristic	Units	Pin Nos.	Min.	Typ.	Max.
Data rate	See note*				
Inputs					
Logic 1 level	volts	see	3.0		5.5
Logic 0 level	volts	diagram	0		0.4
Input loading	unit loads				2-1/2
Switching threshold	volts			2.0	
Outputs					
Logic low level range†	volts	see	-3		-30
Logic high level range†	volts	diagram	0		-0.4
Output current (sinking) (from -3v to -30v)	ma				140
Propagation delay, to 90% of -v (at no load)					
NT33 (to -15v)	ns				500
NT33-1 (to -3v)	ns				250
+5 volt supply (Vcc)	ma	49		60**	70**
+8 volt supply	ma	51		20**	25**
-8 volt supply	ma	50		70**	80**
-v supply	ma	17 depends on -v supply voltage			
example: NT33 at -20v	ma			50**	60**
Dissipation, per module (using example of -v above)	watts			2.02**	2.39**

* Maximum data rate depends on value of rise time control capacitor (C4) and length of cable driven. Data rates range from 100KHz to better than 1MHz.

** At 50% duty cycle.

† Output levels depend on the value of -v that is applied to pin 17. The values given above are the allowable min. and max. values.

LOGIC DIAGRAM



OJ14
MEDIUM DELAY ONE-SHOTS

The OJ14 contains four one-shot circuits (sometimes called single-shots) which produce both Q and $\overline{Q}$ output, of pulse-width that is continuously adjustable from 50 μsec to 2.2 seconds (see Table 1).

The fine adjust pots should not be adjusted to their extremes in order to extend range outside of the normal ranges given in Table 1.

The one-shots trigger on the falling edge of the input pulse. Minimum input pulse is 30 nsec True (high). Output Q goes high typically 75 nsec after input falling edge reaches the +2v switching threshold. Duty cycle is 90%. The output pulsewidth will be increased an indefinite amount if the input is retriggered while the Q output is high.

For a detailed circuit schematic and parts list request OJ14 data sheet.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	KHz		0		18.8
Pulsewidth range			50μs		2.2sec
Duty cycle	%				96*
Inputs					
Trigger	Falling edge of one input, with both initially high for 30 ns min.				
Logic 1 level	volts		3.0		5.5
Logic 0 level	volts		0		0.4
Input loading	unit loads				2-1/2
Switching threshold	volts			2.0	
Outputs					
Logic 1 level	volts		4.5		5.5
Logic 0 level	volts		0		0.4
Fan-out, into DTL	unit loads				
Q outputs		42, 29, 8, 6,			33
$\overline{Q}$ outputs		44, 38, 21, 11			28
Fan-out, into TTL					
Q outputs		42, 29, 8, 6,			27
$\overline{Q}$ outputs		44, 38, 21, 11			27
Propagation delay, at 25°C	ns			75	
+5 volt supply (Vcc)	ma			185	204
+8 volt supply	ma			120	132
Dissipation, per module	watts			1.88	2.28**

* 5% reduction in pulsewidth at max. duty cycle
** at 10% above nominal supply voltages

LOGIC DIAGRAM

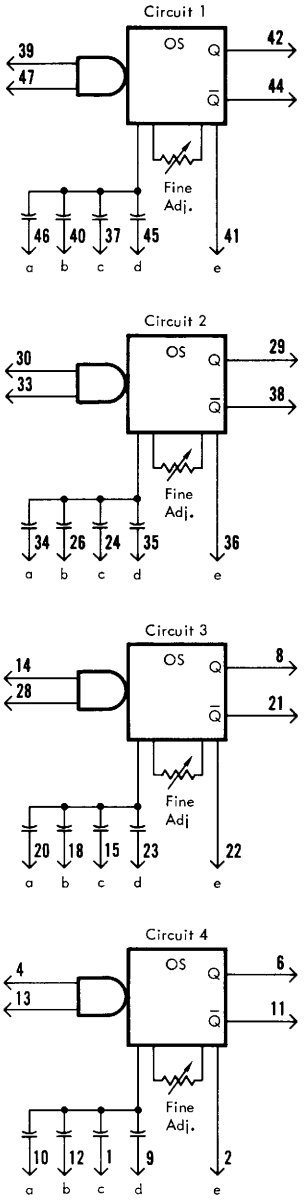
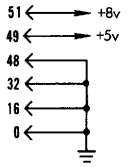


Table 1. Ranges

P. W.	Connect
50-350 μsec	None
0.3 to 3.5 millisec	a - e
3 to 35 millisec	b - e
25 to 300 millisec	c - e
0.2 to 1.5 sec	d - e
0.3 to 2.2 sec	c-d-e



Polarizing keys 10 & 17

OJ18
GENERAL PURPOSE ONE-SHOTS

The OJ18 contains four one-shot circuits (sometimes called single-shots) which produce both Q and $\overline{Q}$ output, of pulse-width that is continuously adjustable from 100 nsec to 20 μsec (see Table 1).

External capacitance may be placed on the module, across standoffs E1 and E2, to extend pulsewidth to as much as 20 milliseconds. The external capacitance value can be determined from the formula p.w. = 1.3C, where p.w. is in milliseconds and C is in μf.

The fine adjust pots should not be adjusted to their extremes in order to extend range outside of the normal ranges given in Table 1.

The one-shots trigger on the falling edge of the input pulse. Minimum input pulse is 50 nsec True (high). Output Q goes high typically 45 nsec after input falling edge reaches the +2v switching threshold. Duty cycle is 50%. The output pulsewidth will be increased an indefinite amount if the input is retriggered while the Q output is high.

For a detailed schematic and parts list request OJ18 data sheet.

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		5
Pulsewidth range			100ns		20μs*
Duty cycle	%			50	
Inputs					
Trigger	Falling edge of one input, with both initially high for 50nsec min.				
Logic 1 level	volts		3.0		5.5
Logic 0 level	volts		0		0.4
Input loading	unit loads	44, 46, 28, 26 20, 18, 6, 4			2-1/2
Switching threshold	volts			2.0	
Outputs					
Logic 1 level	volts		4.5		5.5
Logic 0 level	volts		0		0.4
Fan-out, into DTL	unit loads	42, 40, 30, 34, 14, 12, 8, 10			33
Fan-out, into TTL	unit loads				27
Propagation delay, at 25°C	ns			45	
+5 volt supply (Vcc)	ma			215	280
+8 volt supply	ma				65
Dissipation, per module	watts			1.48	1.92

* Pulsewidth can be extended to 20ms with external capacitance (see text).

LOGIC DIAGRAM

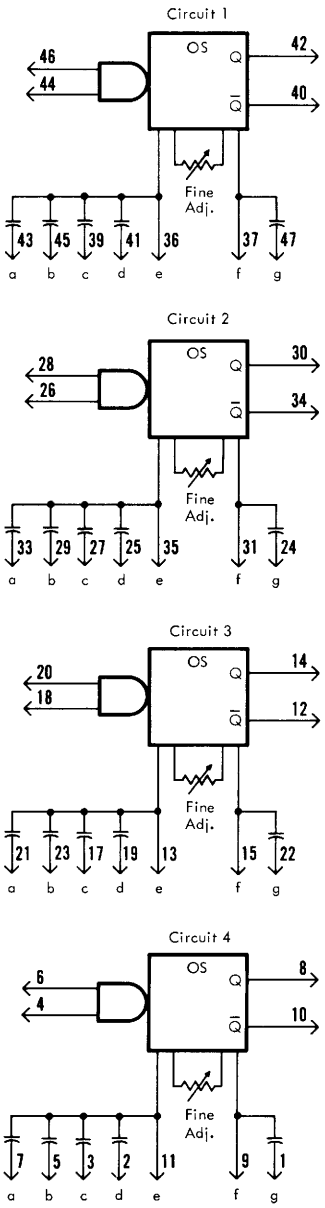
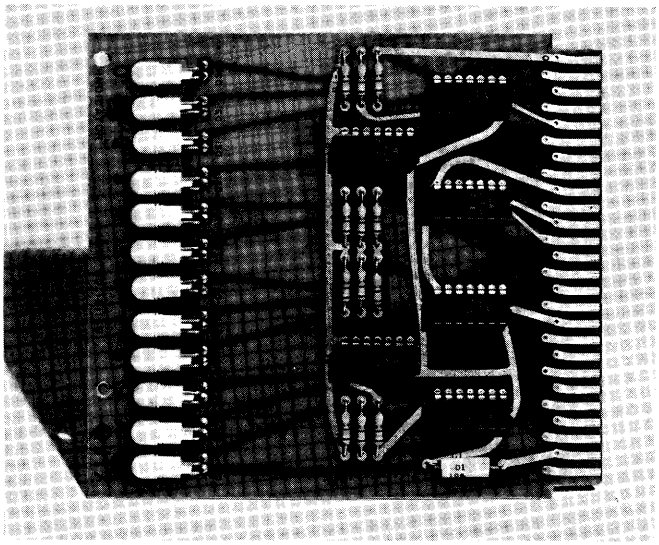


Table 1. Ranges

Jumpers	
P. W. (μsec)	Connect
.10 to .25	None
.25 to .35	d-f
.35 to .50	c-f
.50 to .90	c-d-f
.90 to 1.5	b-g
1.5 to 2.3	b-f
2.3 to 4.7	a-g
4.7 to 8.0	a-f
8.0 to 10.0	a-b-f
10 to 20	a-f, g-e

Polarizing keys 2 & 7

The QJ17 contains twelve indicator lamps driven by an independent NAND driver circuit. Open inputs act as True signals. The "Bright Eye" lamps are clearly visible at distances up to 100 feet.



SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Input loading	unit loads	all inputs			1
+5 volt supply (Vcc)	ma			392†	436*†
Dissipation, per module	watts			1.96†	2.4*†

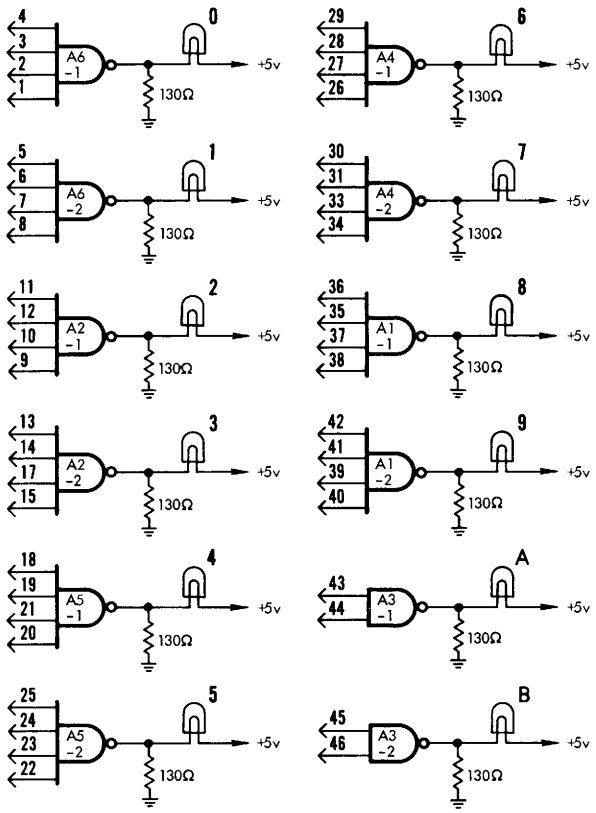
* at +5.5v

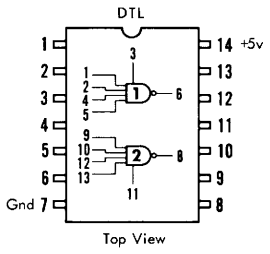
† Does not include bulbs. Add 32 ma max. (176 mw). for each bulb turned on.

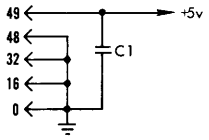
PARTS LIST

Designator	Description	IC Type	Qty.
A1 thru 6	IC power gate	944	6
R1	Res. 130Ω, 1/4w		12
DS1	Lamp, incandescent G.E. type 683		12
C1	Cap., mylar, .01μf		1

LOGIC DIAGRAM







Polarizing keys 2 & 19

RJ10
LAMP AND RELAY DRIVER

The RJ10 module contains eight DTL-gated high-current drivers, suitable for driving either indicator lamps or relays. Each driver can sink up to 200 ma at 28 volts. The flexible input gating can be used to perform 3-input AND functions, AND/OR functions, or storage. When used for storage the input logic is wired as NAND latches (single-output cross-coupled NAND flip-flops). A 3-bit-input decoding network can be constructed to create an octal-output display or relay actuator.

Front edge contacts (double connectors symbol) are provided for an ET11 connector to permit routing of outputs to remote lamps or relays. (The single connector symbols indicate back panel contacts).

An important noise-reduction feature is the provision of an independent common ground for the high-power driver circuits. This ground point is to be connected to system ground.

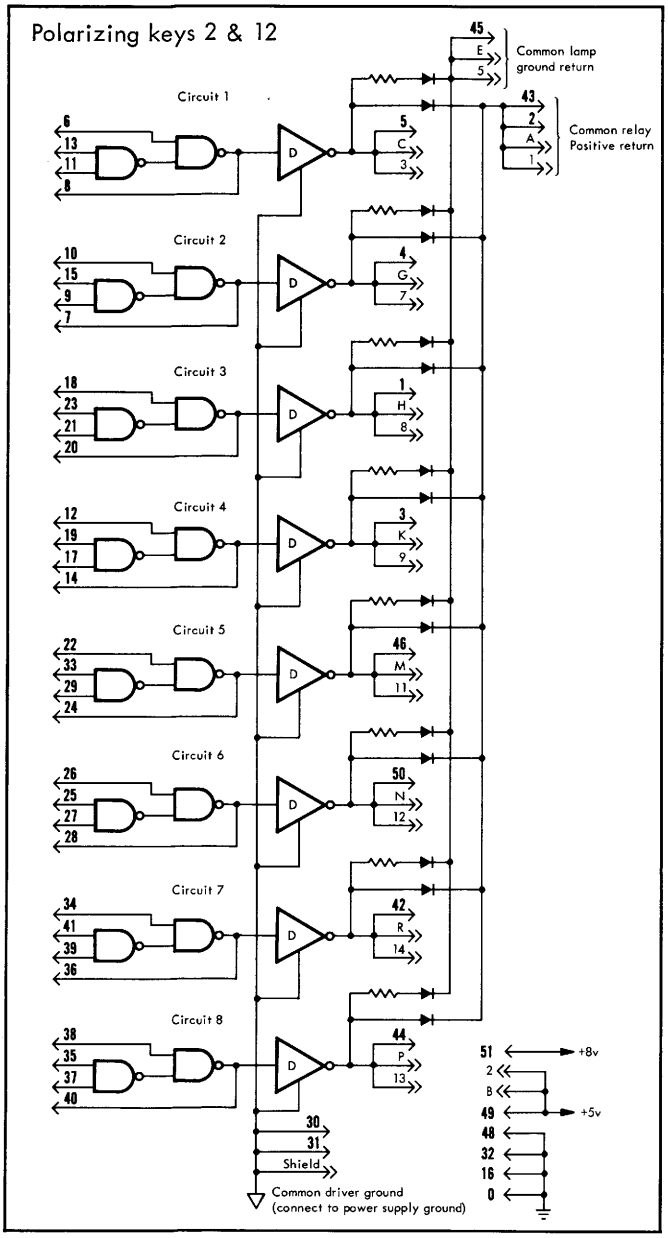
The system engineer can choose either a simple back panel connection for low current applications, via logic wire from pins 30-31 to pins 32 and 48, or a direct connection to power supply ground via heavier gage wire from a shield connection on the ET11 cable connector.

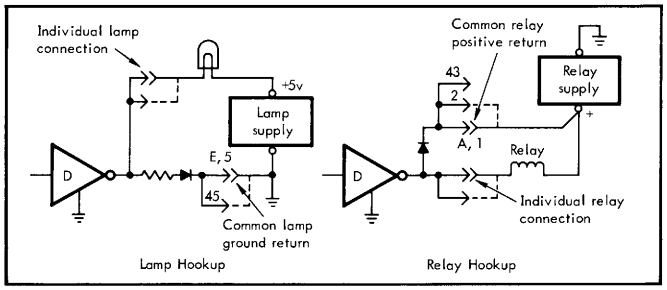
For additional noise protection the driver rise and fall times are deliberately slowed with a Miller integrator, to minimize switching transients.

When a driver is used to operate an indicator lamp the hook-up shown below is used. Note that both front-edge and back panel connections are available. This hook-up also provides a keep-alive resistor to reduce current surge in the output transistor.

For detailed circuit schematic and parts list request RJ10 data sheet.

LOGIC DIAGRAM





SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Clock rate	MHz		0		n.a.*
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Output voltage (externally supplied) Output current (per driver)	volts ma				28 200
Input loading	unit loads	8, 7, 20, 14, 24, 28, 36, 40 All others			11 1
Propagation delay, at 25°C	μs			4	
+5 volt supply (Vcc) +8 volt supply	ma ma			25 132	35 147
Dissipation, per module	watts			1.18†	1.49†

* Not applicable, since load determines maximum switching rate. Refer to propagation delay specification for circuit speed.
† Does not include driver outputs.

The ST14 module contains fifteen independent manually operated single-point-double throw (SPDT) toggle switches. Each switch may be used to apply 0 volts (False) to a J Series logic input. (An open circuit has the same effect as application of +5 volts, or True). The schematic shows the switches in the position of the handle which is marked "1" on the etched circuit board.

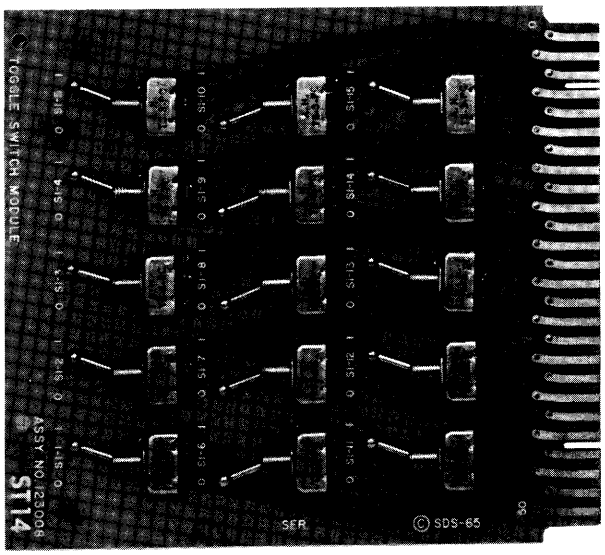
A contact debouncer circuit is shown below. This circuit removes transients due to mechanical bounce of the contacts, and is only needed if switches are to be changed while the system is operating and clock rate is too high to allow the transients to settle.

SPECIFICATION

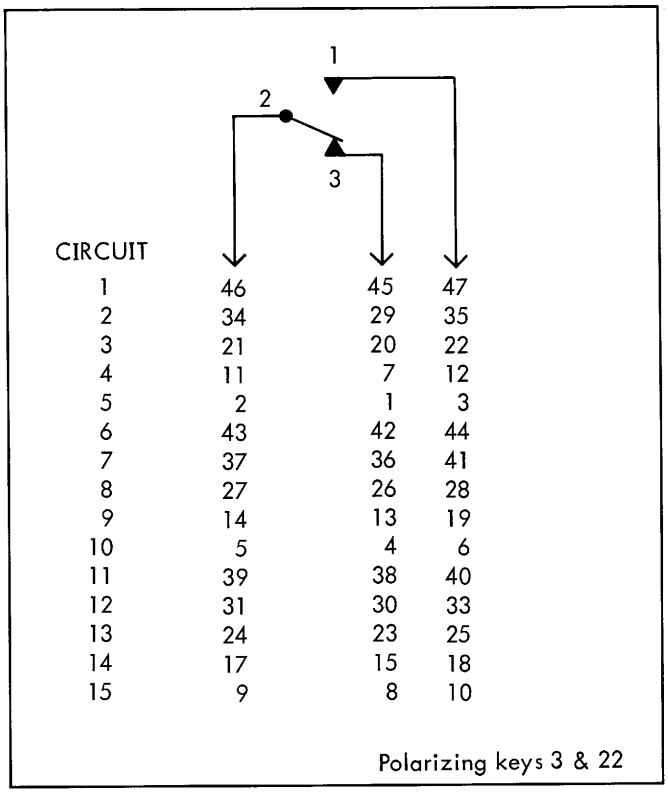
Contact rating	5 amp. at 115 vac.

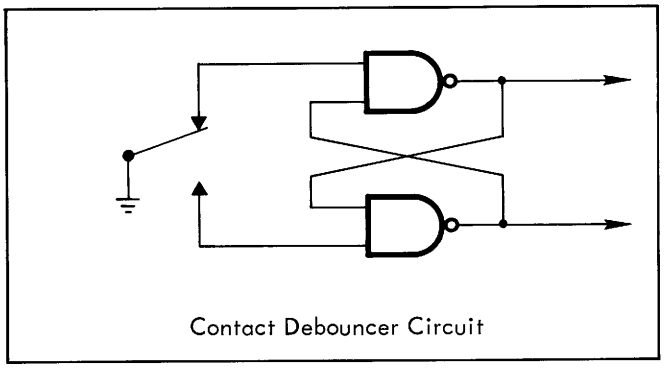
PARTS LIST

Item		Description	Designator	Qty.
1	Switch,	Toggle SPDT	S1	15



SCHEMATIC DIAGRAM





WT49
35V REFERENCE VOLTAGE REGULATOR

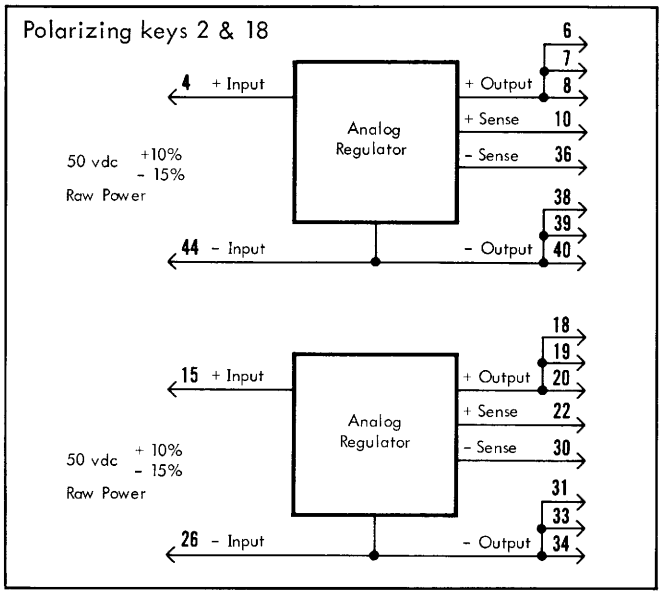
The WT49 module contains two electrically independent precision 35 volt regulators, which have remote sensing capability and are short circuit proof for an indefinite length of time.

Each of the regulators may be used for either plus or minus polarity, much like a battery, by grounding the appropriate side. One WT49 module can supply both +35v and -35v reference voltages for use with digital-to-analog converter modules such as the DJ24. One WT49 module can supply twenty-four DJ24 modules.

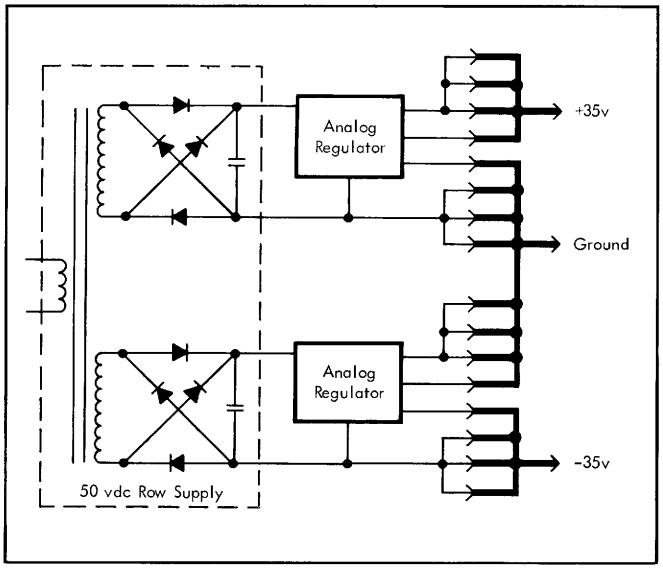
All pins shown below on one input or output should be bussed together on the backplane connector. On long runs use wires in parallel to reduce the current per wire. Where IR drop is expected to be a problem, wire the sense inputs to a representative point in the load. Otherwise wire sense inputs to outputs on the WT49.

The WT49 requires one card slot. However, because of the high dissipation it is advisable to either leave an empty card slot beside the component side, or place a cable-plug or other passive module beside the component side.

For detailed circuit schematic and parts list request WT49 data sheet.



Input-Output Diagram



Connection as ±35 vdc Supply

SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Output voltage Output volt. adjustment Output current, each regulator citcuit (I out)	vdc mv ma	see diagram	 0		35* 3 250
Load regulation	%		±0.03		
Ripple rejection			400:1		
Temperature coefficient (from 0°C to +55°C)	%/°C				0.003
Operating temperature range	°C		0		+55
Input voltage range† (Vin) Input current	vdc ma	see diagram	40		55 300
Dissipation, per module	watts				12.5

* Either polarity.
† Isolated from ground. May be obtained from PT23 or PT26 supply.

WT53, WT54
25V AND 15V REFERENCE VOLTAGE REGULATORS

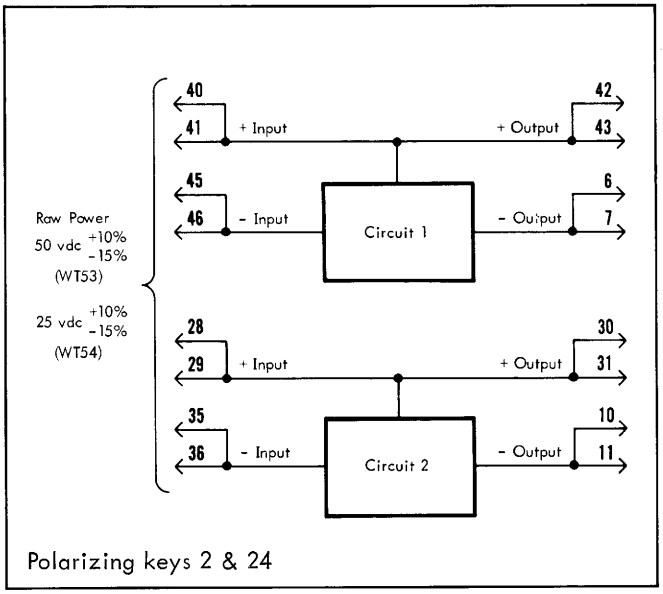
The WT53 and WT54 each contain two electrically independent precision regulators, which are short circuit proof for a period of 30 seconds. The WT53 delivers ±25 volts, while the WT54 delivers ±15 volts.

Each regulator circuit may be used for either plus or minus polarity, much like a battery, by grounding the appropriate side. Thus one module with its two independent regulator circuits can supply both + and - reference voltages (see connection diagram).

All pins that are shown on one input or output should be bussed together on the backplane connector. On long runs use parallel wires from the regulator to the destination to reduce IR drop.

One regulator module requires two card slots. However, because of the high dissipation it is advisable to either leave an empty slot beside the component side, or place a cable-plug or other passive module beside the component side.

For detailed circuit schematics and parts list request WT53, WT54 data sheet.



Input-Output Diagram

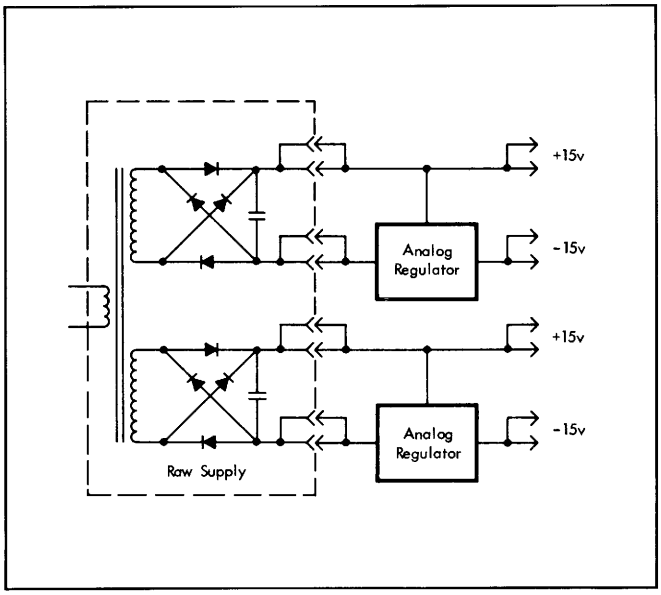
SPECIFICATIONS

Characteristic	Units	Min.	Typ.	Max.
Outputs				
WT53 nominal output voltage†	vdc		25	
WT53 voltage adjust resolution	mv	±40		
WT53 output current, each ckt. (I out)	amp.			0.4
WT54 nominal output voltage†	vdc		15	
WT54 voltage adjust resolution	mv	±20		
WT54 output current, each ckt. (I out)	amp.			1.0
Load regulation	%	1		
Ripple rejection		50:1		
Temperature coefficient (from 0°C to +55°C)	%/°C			0.05
Operating temperature range	°C	0		+55
Inputs				
WT53 input voltage range* (for nominal outputs)	vdc	29	49	55**
WT53 input current	amp.			0.55
WT54 input voltage range* (for nominal output)	vdc	19	22.5	26**
WT54 input current	amp.			1.2
Dissipation, per module	watts			24

† Output voltage can be adjusted over a range of ±2.5 volts on WT53, and ±2 volts on WT54.

* Isolated from ground. May be obtained from PT23 or PT26 supply

** Do not use this value of maximum input voltage under maximum current load.



WT54 Connection Diagram

XJ10
EXTERNAL PULL-UP RESISTORS FOR DTL

The XJ10 module contains forty-six 1.1K ohm resistors, each connected between a separate module contact and +5 volts. A single 1.1K ohm resistor can be connected, via logic wire, to a J Series DTL output. Such a connection places the 1.1K ohms in parallel with the integrated 6K ohm pull-up resistor on the DTL chip, reducing the fan-out by 3 DTL unit loads.

Decreasing the pull-up resistance in this manner speeds up the rise time and therefore decreases propagation delay.

External pull-ups are usually not required with DTL logic at clock rates under 1 MHz and with logic wire lengths less than 20 inches. They should always be used, however, at the ends of clock distribution lines in DTL systems, to assure fast clock rising edges and provide a better impedance match than is provided by an open circuit, thus reducing reflections.

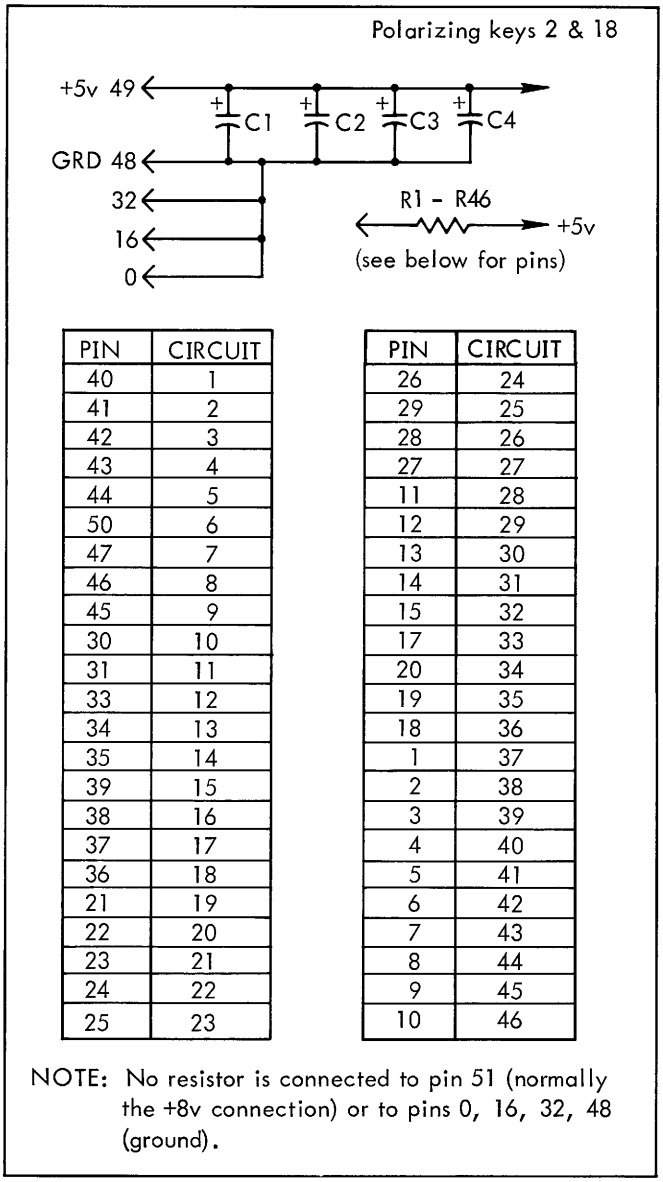
SPECIFICATIONS

Resistance of each resistor	1.1K ohms, ±5%, 1/4 watt
Current through each resistor when output transistor is turned on	4.8 ma (3 unit loads)

PARTS LIST

Designator	Description	Type	Qty.
R1 thru R46	Resistor, Fixed Film, 1.1K ohm, ±5%, 1/4w		46
C1, 2, 3, 4	Capacitor, Tantalum 12µf, ±20%, 15v		4

SCHEMATIC DIAGRAM



PIN	CIRCUIT
40	1
41	2
42	3
43	4
44	5
50	6
47	7
46	8
45	9
30	10
31	11
33	12
34	13
35	14
39	15
38	16
37	17
36	18
21	19
22	20
23	21
24	22
25	23

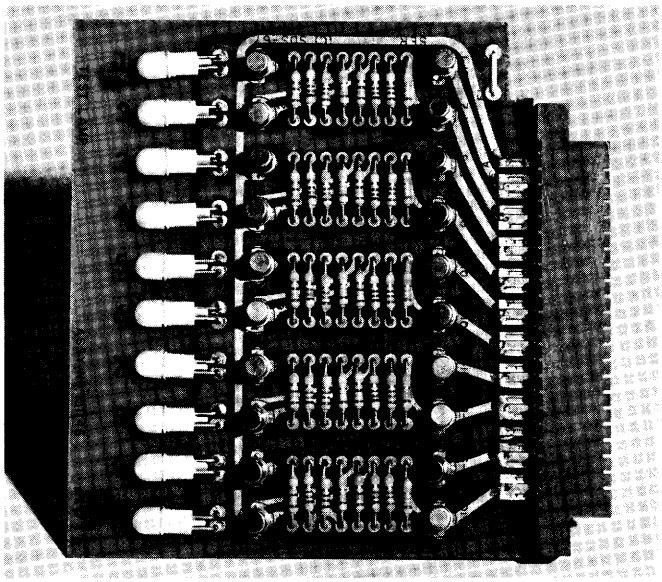
PIN	CIRCUIT
26	24
29	25
28	26
27	27
11	28
12	29
13	30
14	31
15	32
17	33
20	34
19	35
18	36
1	37
2	38
3	39
4	40
5	41
6	42
7	43
8	44
9	45
10	46

NOTE: No resistor is connected to pin 51 (normally the +8v connection) or to pins 0, 16, 32, 48 (ground).

XJ11
TEST LAMP ASSEMBLY

The Test Lamp Assembly plugs on the front edge of any J Series module that has test points on the front edge. The XJ11 contains ten independent test lamp circuits on a module with a special connector mounted at the back. Each lamp circuit input connects to one test point on the module under test.

The XJ11 conveniently allows the user to visually troubleshoot without incurring the cost involved in placing test lamps on logic modules in the system. The logical states of all lamps are visible simultaneously.



SPECIFICATIONS

Characteristic	Units	Pin No's.	Min.	Typ.	Max.
Logic 1 level Logic 0 level	volts volts		2.6 0		5.5 0.4
Switching threshold	volts			1.5	
Input loading	No loading when circuit under test is in current sinking (logic 0) condition. Drops high logic level by no more than 20% when circuit under test is in logic 1 condition.				
+5 volt supply (Vcc)	ma			280†	310*†
Dissipation, per module	watts			1.4†	1.7*†

* at +5.5v

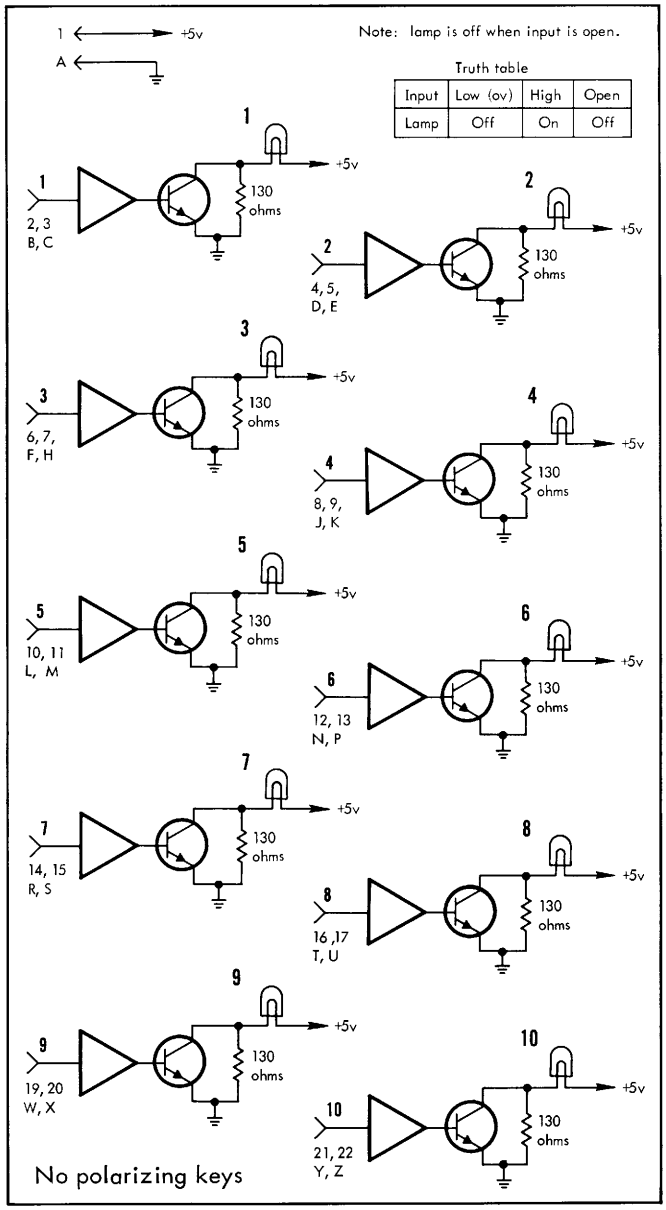
† Does not include bulbs.
Add 36 ma max. (197 mw) for each bulb turned on.

The XJ11 circuit is designed to load the circuit under test as little as possible in the logic 0 (current sinking) condition, by providing a high impedance input.

Avoid connecting the Test Lamp Assembly to highly loaded DTL outputs which drive TTL inputs, to prevent pulling logic 1 voltage below the minimum acceptable +2.6 volt logic level with the additional load of the test lamp circuit.

For detailed schematic and parts list refer to XJ11 data sheet.

LOGIC DIAGRAM

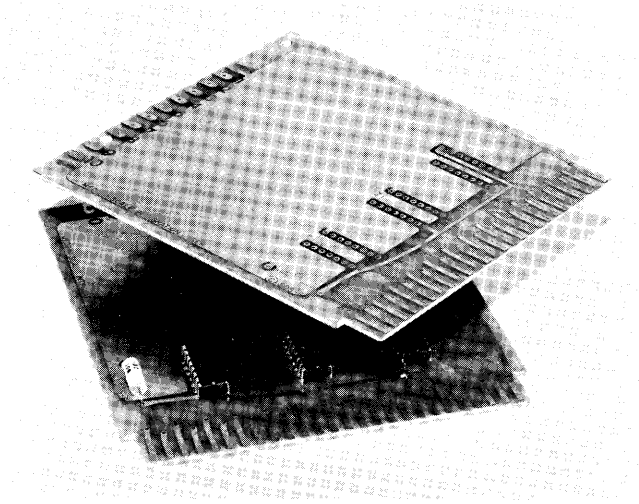


XJ12, XJ13
MSI BREADBOARD MODULES

The XJ12 and XJ13 are etched circuit boards, drilled for mounting three 16-lead dual-in-line MSI circuits. The etch pattern on one side connects all of the leads from each MSI circuit position to back panel connector pins at the back edge of the board. The etch pattern on the other side of the board forms a ground plane. No circuit components are provided.

On the XJ12, ground connection is made to pin 8 of each IC, and Vcc connection to pin 16. On the XJ13, ground connection is made to pin 12 of each IC, and Vcc connection to pin 5.

XJ12 polarizing keys are placed at positions 2 and 22.
XJ13 polarizing keys are placed at positions 3 and 12.



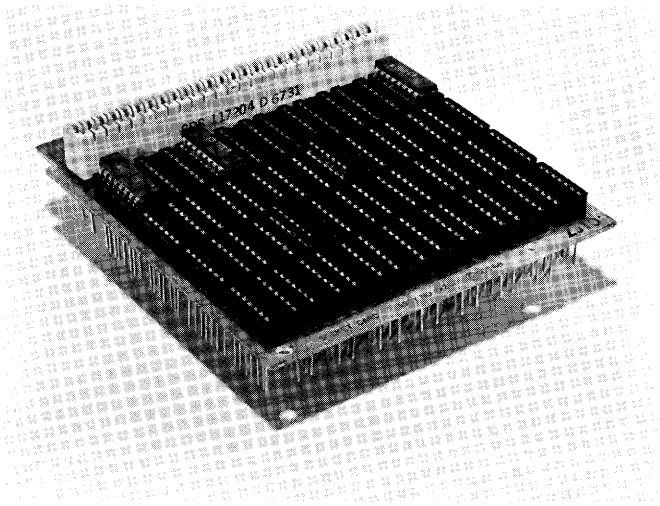
XJ12 Blank Module

ZJ10
SOCKET MODULE

The ZJ10 Socket Module provides dual-in-line sockets to enable the user to mount up to eight 16-lead and twenty-four 14-lead dual-in-line packages, or thirty-two 14-lead packages, without soldering leads to the board. Each lead is connected to a wire-wrap pin which is accessible on the opposite side of the board. These wrap posts can be individually connected to the back-panel connectors along the back edge of the board.

The ZJ10 module allows the user to build, and change, a subsystem on one module. The ZJ10 requires three card slots.

ZJ10 polarizing key is placed at position 2.

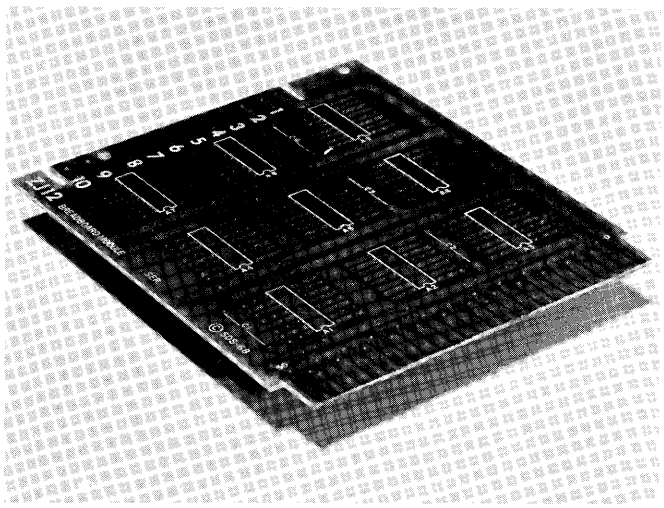


ZJ10 Socket Module

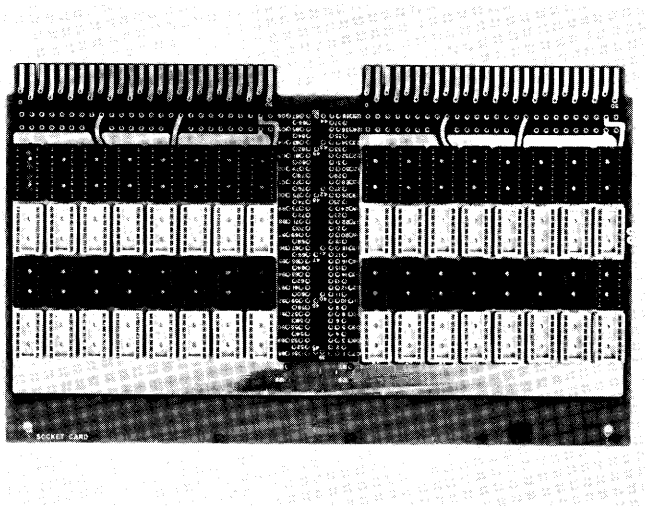
ZJ12
DUAL-IN-LINE BREADBOARD MODULE

The ZJ12 is an etched, drilled module, without components. Space is provided to insert nine 14-lead or 16-lead dual-in-line packages and decoupling capacitors. The circuits are soldered to the etch pattern, and interconnections are made with jumper leads soldered in place. Etched circuit pads are provided for each lead, and for ground and Vcc connections.

ZJ12 polarizing key is placed at position 2.



ZJ12 Dual-in-line Breadboard Module



ZJ14 Double Height Socket Module

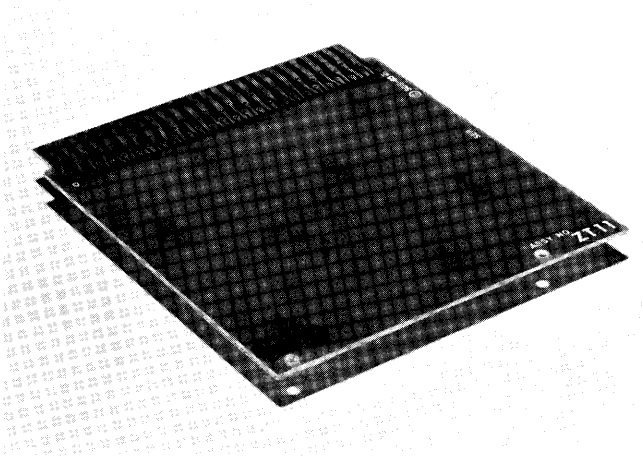
ZJ14
DOUBLE-HEIGHT SOCKET MODULE

The ZJ14 module provides sixty-four sockets, to hold forty-eight 14-pin dual-in-line ICs and sixteen 16-pin dual-in-line ICs, or sixty-four 14-lead ICs. Each contact in each socket connects to a wire-wrap post which is accessible on the opposite side of the board. The signals which are to leave the board are wrapped to the module connectors along the back edge via the two sets of 52 wrap posts available on the specially mounted backplane connectors.

The ZJ14 mounts in a model MT42 two-high mounting case, and occupies three card slots.

The VT10 jumper kit, described in Section 3, provides a convenient method of temporarily interconnecting wrap pins.

ZJ14 polarizing keys are placed at position 2 in both upper and lower locations.



ZT11 Blank Module

ZT11
BLANK MODULE

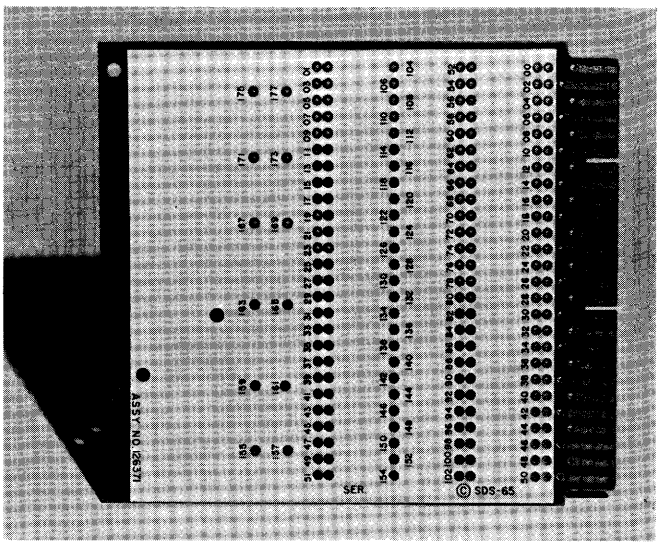
The ZT11 Blank module is useful when building special circuits with discrete components which vary in size, where interconnections will be made with jumper wires. The module consists of an undrilled epoxy-glass board with gold-plated copper foil ribbon connectors along the back edge, but no other copper foil.

ZT11 has no polarizing key slot.

ZT15
CABLE-PLUG MODULE
(SOLDER CONNECTIONS)

The ZT15 will accept up to 44 shielded conductors: one 30-conductor cable and one 14-conductor cable, which are fastened to the front edge with a plastic cable clamp. All conductors and shields should be soldered to the etch provided. Extra mounting holes and interconnecting etch are provided for optional component mounting. The ZT15 is most useful for low-frequency work (under 2 MHz) where the effects of parasitic capacitance are not important and noise levels need not be kept to a minimum.

ZT15 polarizing keys are placed at positions 6 and 15.



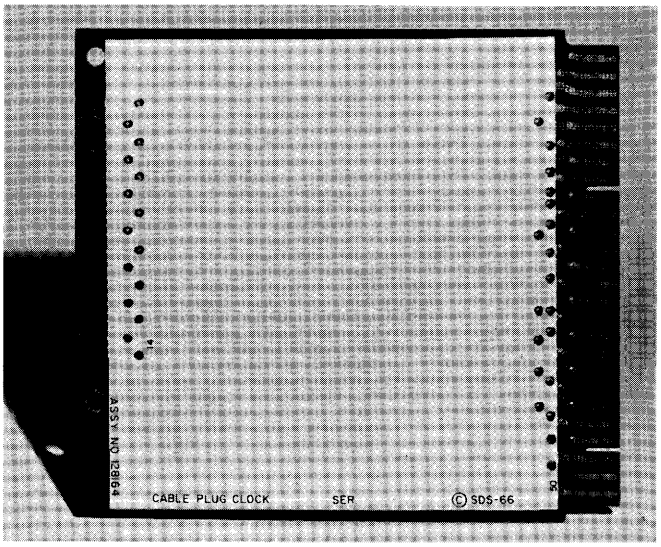
ZT15 Cable-plug Module

ZT23
CABLE-PLUG MODULE
(FRONT-EDGE CONNECTIONS)

The ZT23 module is designed to accept up to 28 individually shielded conductors, which can be connected as two bundles of 14 cables each to the front edge of the module, using two of the Model ET11 cable connectors. Model ET12 cable is recommended. Model ET10 or ET14 pre-assembled cables with connectors are usually employed.

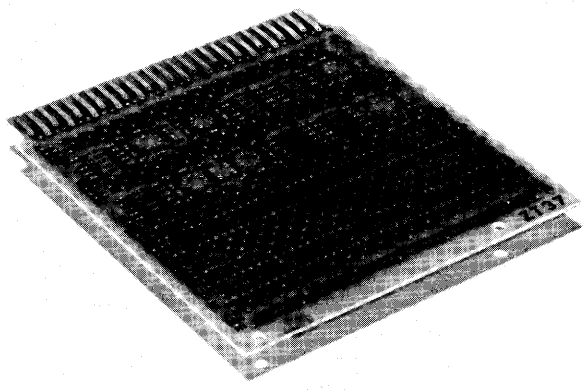
A straight-through etched circuit pattern on each side routes signals from the front edge to the back-panel edge of the card. Connections to one side of the module front edge are independent of connections to the other side, and the two etched patterns are separated by a ground plane through the center of the module which acts as a shield.

ZT23 polarizing keys are placed at positions 8 and 23.



ZT23 Cable-plug Module

ZT37
BREADBOARD MODULE

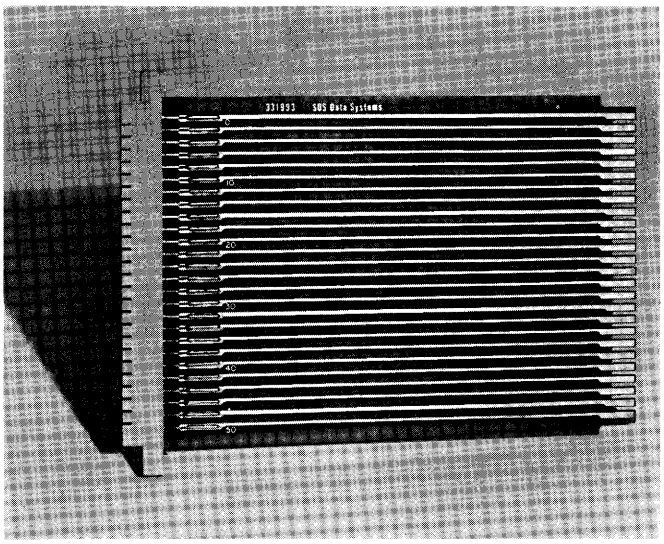


ZT37 Breadboard Module

The ZT37 Breadboard Module has a versatile etch circuit pattern arranged for convenient mounting of all standard components, including diodes, capacitors, resistors, transistors or IC's in TO-5 cans, flat packs, or the 14-lead or 16-lead dual-in-line package. This module permits custom building of special circuits while retaining the advantages and mechanical compatibility of J Series etch circuit construction.

The ZT37 differs from the ZJ12 in that the ZT37 accommodates a variety of solid-state component packages, while the ZJ12 is specialized to handle dual-in-lines.

ZT37 has no polarizing key slot.



ZT53 Extender Module

ZT53
EXTENDER MODULE

The ZT53 Extender Module has a straight-through etched circuit pattern and a VT12 connector mounted on its front edge. It permits the user to extend any module in front of the rack so that circuit operation may be investigated while the module is plugged into the system. Contacts are Rhodium plated for long life. ZT53 has polarizing slots in all positions.

ZT60
COPPER-CLAD BLANK MODULE

The ZT60 Copper Clad blank is similar to the ZT11, but has solid sheets of gold-plated copper foil attached to both sides. The board can be drilled and etched as desired. It is useful for making limited production runs of special modules. ZT60 has no polarizing key slot.

ACCESSORIES AND SERVICES

OTHER ESSENTIAL COMPONENTS OF A MODULE FAMILY

SDS offers a full line of accessories, mounting hardware, and tools. Their use eliminates mechanical design cost, reduces procurement lead time, and reduces assembly time. SDS also offers a full range of services and documentation that save engineering time.

The accessories are identical to those offered with the T Series high performance (10 MHz) module line, as used in SDS Sigma computers.

Accessories include:

1. Cabinets with doors, optional side panels, ac power connectors, and optional swing-out mounting case containers (swing frames).
2. Individual 32-module mounting cases, and 3-case 90-module drawer; with hinged doors or fixed panels to cover mounting cases or to fill blank spaces.
3. Two-high mounting case with spaces for five double-height socket boards and 32 standard size modules.
4. Blower assembly for cooling.
5. Compact power supply.
6. Cable connectors and cables, and cable-plug modules.
7. Spooled wire, cut-wire jumper kits, wiring tools, and individual module connectors.
8. Accessory modules for breadboard and trouble-shooting.

These cost-reducing services are also provided:

1. Automated Wire Listing (AWL)
2. Automated Wiring Service (AWS)
3. Application engineering by experienced computer engineers and by technically oriented sales engineers.
4. SDS designed and built special-order modules, made to your specifications at reasonable cost.
5. Thorough documentation.
6. Fast, off-the-shelf delivery of new modules or spares.
7. Module repair facility.
8. One-year warranty on all SDS products.

ACCESSORIES

DETAILED SPECIFICATIONS

Full specifications and detailed drawings for the accessories described below are given in SDS catalog 64-51-15.

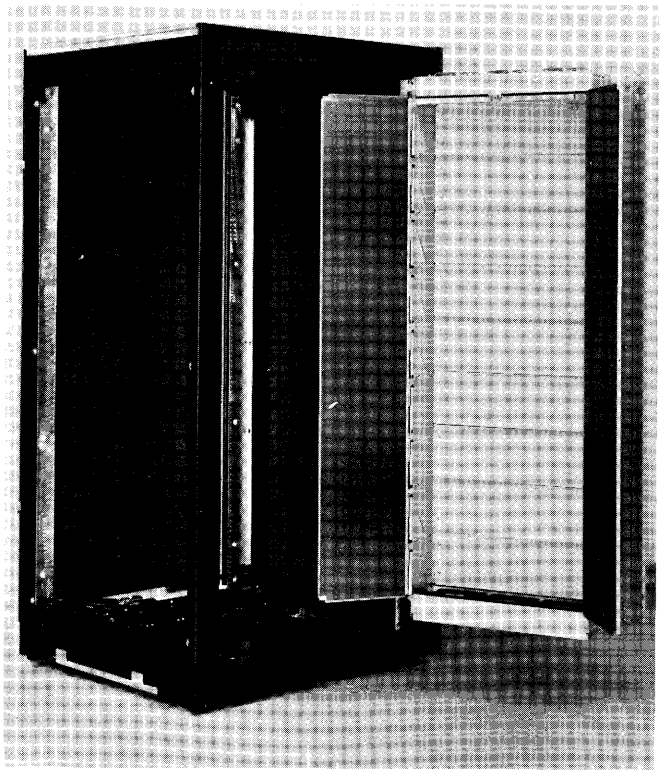
YT19, YT24, and YT14 CABINETS

Three types of cabinets are available, all with outside dimensions 63-3/8 inches high (including casters), 29-1/2 inches wide (without side panels) and 31-5/8 inches deep (with back door).

One cabinet, Model YT19, is made for mounting of individual 19-inch wide, 32-module mounting cases, power supplies and blowers. A vertical control panel is included. The cabinet also contains ac power outlets, a circuit breaker, a local/remote switch, dc wiring junctions and a power cord. Top and bottom have protective grills. Side panels (Model YT30) are optional. An insulated, soundproof hinged back door is standard.

A 24-inch version of this versatile system cabinet is available as Model YT24. The YT24 is ideal for use with 3-high and 7-high swing frames.

A third type, Model YT14 (shown below), is designed to mount one or two swing frames which can each hold three, seven, or nine individual mounting cases, plus blowers. The swing frames contain the blowers, and also have front panel covers in place for unused mounting case spaces. Double doors (shown open) completely enclose the mounting cases. Hinged back door, ac power sockets, and ac power cord are included in the YT14 cabinet. Side panels (Model YT30) are optional. Swing frame model numbers are YT43 (3-high), YT47 (7-high), and YT49 (9-high).



MT SERIES MOUNTING CASES

MT10, MT12, MT30, and MT32 Cases

Standard cases accomodate 32 modules, are 5.25 inches high, 7.90 inches deep, and fit into a standard 19-inch width rack. Wiring terminals are either solder tail or wire wrap. Each case comes with connectors, +4v and +8v power wiring, and ground plane installed.

Four combinations of fixed or hinged mounting, and the two pin types are available:

1. Solder terminals, fixed mount: MT10
2. Solder terminals, vertical hinge, right or left: MT30
3. Wire-wrap terminals, fixed mount: MT12
4. Wire-wrap, vertical hinge, right or left: MT32

All cases can be mounted with pins toward either front or back of cabinet. All brackets and hinges are adjustable and reversible, front-to-back and left-to-right. Cable troughs and pin protectors are standard on all mounting cases.

MT13 and MT33 Cases

The MT13 (fixed mount) and MT33 (hinged mount) cases are similar to MT10/MT12 and MT30/MT32 cases, but are without the backplane/connector assembly. These cases facilitate combination of special equipment with J Series modules in the same assembly. The user provides his own connectors, ground and power bussing, etc.

MT42 Two-high Case

The latest addition to the SDS line of mounting cases is model MT42, designed to hold both double-height socket boards (ZJ14) and standard size modules, as well as the compact PT10 power supply.

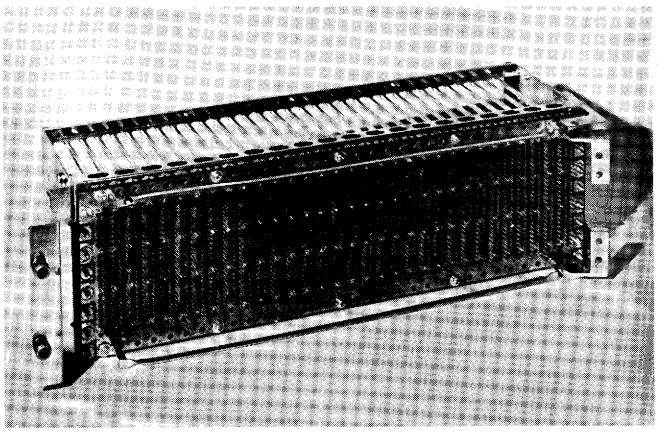
MTD1 and MTD2 High Density Cases

The MTD1 and MTD2 high density drawer-type mounting cases each contain three basic card cages with power and ground planes, identical to those used in the mounting cases described above, mounted in a drawer with tiltable slides which use ball-bearing rollers. Each case holds up to 90 modules, is 8.73 inches high, 22.03 inches deep, and fits into a standard 19-inch rack.

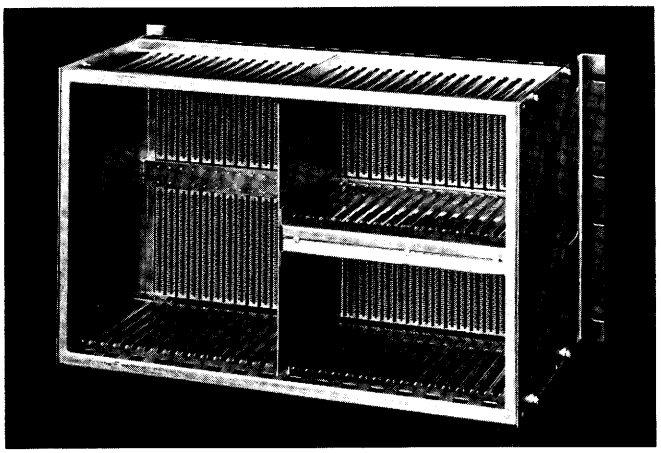
The slides allow the drawer to extend full depth from the cabinet and to be tilted in 45° increments over 180° from drawer-front point up, to pointing down.

A ZT20 blower with washable air filter is included. All power and ground connections to the three card cages are brought out to a terminal board. A module locking bar is provided for each card cage, and both top and bottom protective covers are furnished.
Panel mounted indicators and switches can be mounted behind the 1.09 inch deep front panel, which comes with two folding handles and captive fastening screws.

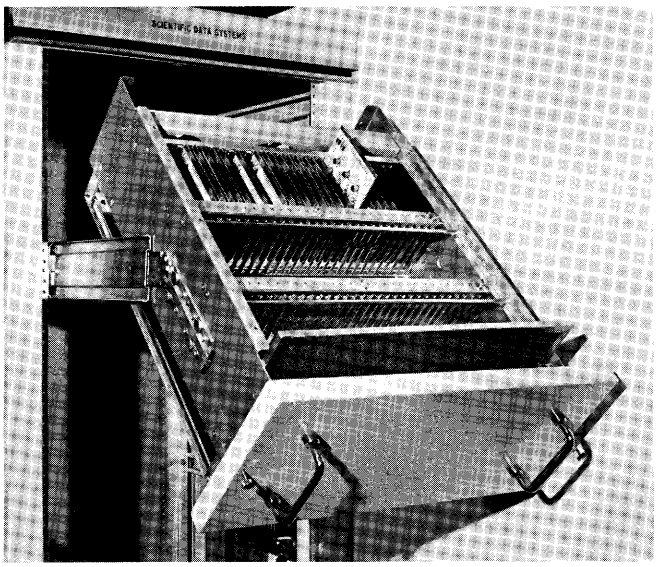
The MTD1 case has solder-tail terminals while the MTD2 has wire-wrap terminals.



MT32 Hinged-Mount Case, Showing Ground Plane



MT42 Two-high Mounting Case



MTD1 High-Density Drawer Mounting Case

ZT SERIES DOORS

Three 19-inch wide hinged doors, reversible left or right, are available. Each door has a spring loaded latch at the end opposite the hinge. Indicator lamps, switches, meters, and connectors can be mounted in the doors.

Model ZT17	5-1/4 inches high (covers one MT series case*)
Model ZT18	10-1/2 inches high (covers two MT series cases*)
Model ZT19	15-3/4 inches high (covers three MT series cases*)

* except MTD1, MTD2, which have built-in front panels

Four 19-inch wide cover panels are also offered:

Model ZT40-1	1-3/4 inches high
Model ZT40-2	3-1/2 inches high
Model ZT40-3	5-1/4 inches high
Model ZT40-4	7 inches high

ZT20 BLOWER ASSEMBLY

The Model ZT20 Blower Assembly includes a housing which contains three 100 cfm muffin fans mounted side-by-side, three finger guards, a washable air filter, and mounting brackets. The entire assembly is 19-inches wide, 3-1/2 inches high, and 7-inches deep, and mounts with the fan blades turning in a horizontal plane. One ZT20 assembly delivers 300 cfm.

POWER SUPPLIES

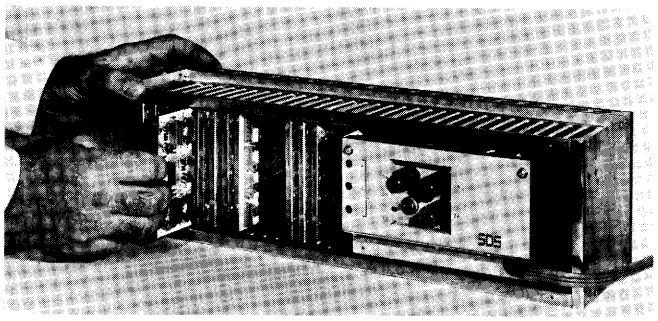
Model PT10 Compact Supply

Model PT10 fits into any MT mounting case, occupying 15 slots. It can power from 20 to 40 modules depending on load. Included are output voltage adjustments and protection against short circuits and overvoltage. Retainers are provided to lock the supply into the mounting case. The supply may be mounted in any position.

Input: 47 to 66 Hz, 1ϕ, 100 vac to 230 vac

Outputs: +5 vdc, 8 amp. (40 va)
+8 vdc, 2 amp.
-8 vdc, 0.6 amps
22 vac, 1/2 amp.
} Regulation: ±5%

Weight: 12 lbs.



PT10 Compact Power Supply Installed Beside Logic Modules

PT23 and PT24 Digital/Analog Power Supplies

The PT23 and PT24 Supplies provide power for a typical 32-module analog chassis, such as the SDS MD51 Multiplexer-Digitizer, or the DA40 D-to-A Converter. Each consists of a PT10 logic voltage supply and a separate analog voltage supply, designed for compact 19-inch mounting.

PT23	PT24
Input (47-66Hz, 1ϕ)	
115 vac ±10%, 225 watts	115 vac ±10%, 570 watts
Outputs	
+5 vdc, 8 amp[t], +8 vdc, 3 amp, -8 vdc, 0.6 amp } ±5% reg. *50 vdc, 0.45 amp, *50 vdc, 0.45 amp } unreg. +15 vdc, 1 amp, -15 vdc, 1 amp } ±1% reg.	+5 vdc, 8 amp[t], +8 vdc, 2 amp, -8 vdc, 0.6 amp } ±5% reg. +25 vdc, 2.5 amp, -25 vdc, 2.5 amp } ±0.5% reg.
* floating [t] Adjustable to 4 volts for T Series operation	
Weight	
50 lbs.	50 lbs.
Panel Height	
5-1/4 inches	5-1/4 inches

PT26 Analog Power Supply

The PT26 Supply consists of the analog supply portion of the PT23, but does not include the logic voltage supply section of the PT23. Specifications of the PT26 are:

Input: 47-66 Hz, 1ϕ, 115 vac ±10%, 125 watts	
Outputs:	
50 vdc, 0.45 amp. (floating), 50 vdc, 0.45 amp. (floating) } unreg.	
25 vdc, 1.2 amp. (floating), 25 vdc, 1.2 amp. (floating) } unreg.	
Weight: 25 lbs.	Panel Height: 3-1/2 inches

CABLING COMPONENTS

ET Series Coaxial Cabling Components

These coaxial cabling components minimize noise pickup and signal distortion, and simplify the mechanical aspects of cabling. The mechanical arrangement is shown in the diagram on pg. 117. Each MT series mounting case has a cable trough attached to its bottom edge. Several fourteen-conductor 33 ohm coaxial cables (Model ET12) may be placed side by side in the trough. The shields and inner conductors of each cable are individually soldered to fourteen common ground points and fourteen independent signal points on a front-edge cable connector (Model ET11). Another ET11 Cable Connector is tied to the end of another cable and the

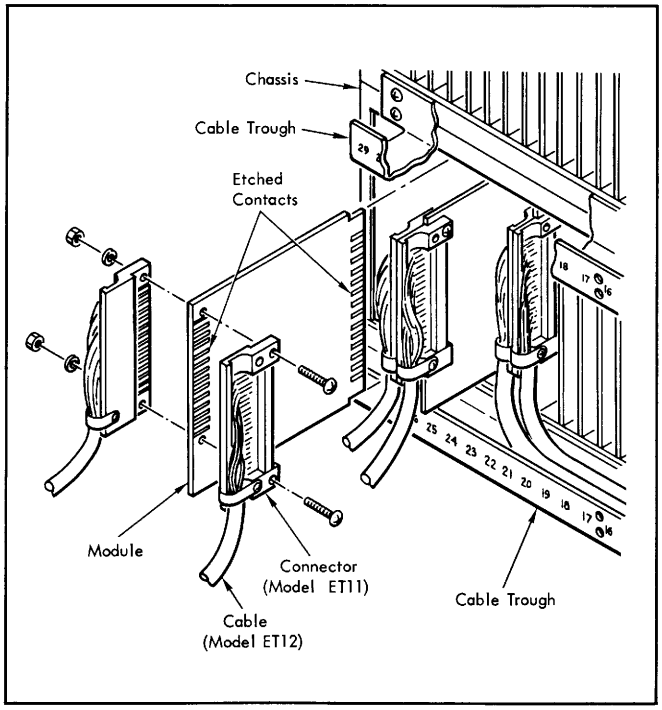
two ET11's are bolted together, through holes in the front edge of an appropriately etched module. A pressure contact is made between the contacts on the ET11's and the module etch.

A preassembled cable-with-connectors assembly, using ET12 Cable and an ET11 Cable Connector at each end, is available as Model ET10-XX, where XX specifies the length of cable in feet.

A preassembled cable-with-connector assembly with an ET11 at only one end, using ET12 Cable, is available as Model ET14-XX-Y. Here, XX specifies length in feet and Y defines whether the ET11 is to be mounted on the etch side (normally left side) of a module or on the component side. Y = E for etch, C for component.

A Model ET13 Dummy Load must be placed at the end of a cable run to properly terminate the run. This item consists of an ET11 Connector which has fourteen 33 ohm resistors soldered between the fourteen ground and fourteen signal connection points.

Modules which are designed to accept ET11 connectors have front-edge contacts, twenty-eight on each side, fourteen connected together to ground and fourteen independent for signal connections. On most module types the ground and signal connections on one side are connected to corresponding etch connectors on the other side by plated-through holes. On some modules they are independent. Typical modules which have the front-edge contacts are: AJ10, AJ11, AJ12, RJ10, and ZT23. When ET11 Cable Connectors are attached, these modules cannot be located in adjacent module spaces, but a module of another type may be placed in the intervening slot.



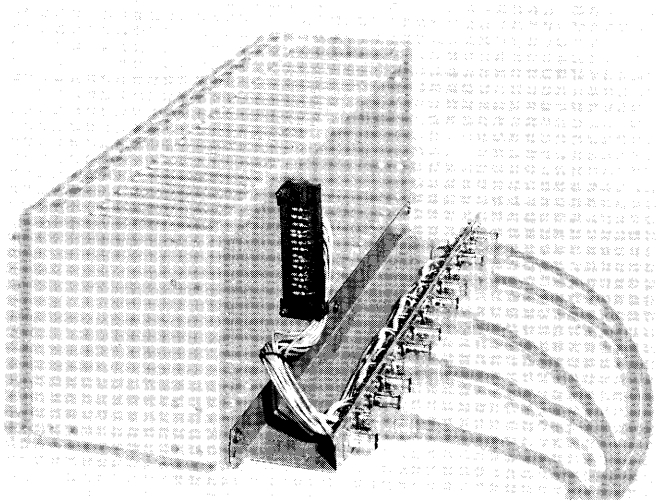
Cable Component Details

ET24 BNC Connector Tray

The ET24 is a 14-coax to module-front-edge connector assembly. It is designed to connect up to fourteen RG62A/U (93-ohm) coaxial cables with AJ10, AJ11, and AJ12 cable driver/receiver modules, when high-speed transmission of data is desired over distances from 200 ft. to 3,000 ft. or more. The maximum data rate at 3,000 ft. is 5 MHz. It can also be conveniently used to connect noise sensitive inputs, such as low-level-analog, to an amplifier module in a mounting case.

The ET24 includes a cable tray which has a row of fourteen silver-plated BNC connectors mounted on its front edge (see photo, below). A shielded single-conductor cable is wired to the standoff side of each BNC connector, and all fourteen individual shielded cables are connected at their other ends to an ET11 connector. Terminating load resistors of 93 ohms each are provided on a second ET11 connector which is clamped to the other side of the receiving module. The cables between the BNC connectors and the ET11 connector are cut to lengths which allow the ET11 connector to be placed anywhere in the mounting case.

When used for long-line transmission with 93 ohm cables, only one set of cables can be connected to the sending and receiving modules; chaining is not allowed.



ET24 BNC Connector Tray

ZT45 and ZT46 Ribbon Cable Assemblies

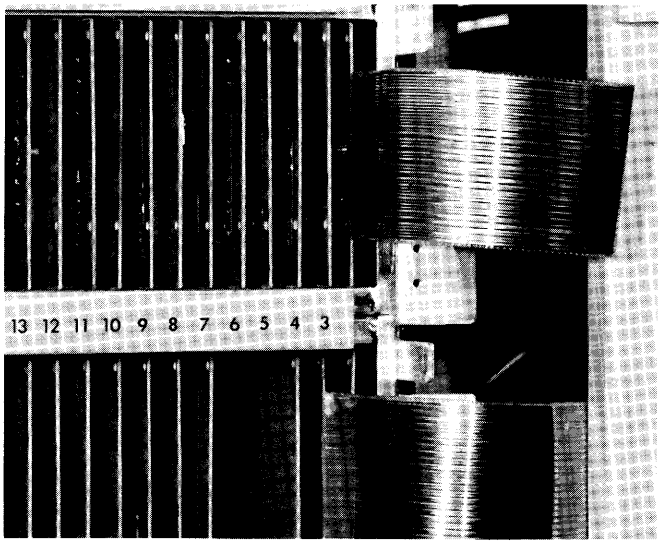
The ZT45 and ZT46 Ribbon Cable Assemblies use a flexible cable containing fifty-two copper foil conductors embedded in a durable ribbon of Teflon approximately 3 inches wide. Two such ribbons are sewn together, forming a cable with a total of fifty signal conductors and fifty-four ground conductors. The ends of each conductor are soldered to a pair of etched-circuit board plugs which plug into any slot in a mounting case.

The ZT46 cable assembly has the circuit board plug long axis oriented in parallel with the cable axis, allowing the ribbon cable to enter a module mounting case from the front, as shown below. The ZT45 cable assembly has the plug axis at right angles to the cable axis. This allows entry of the ribbon cable vertically into a mounting case through a ventilating slot, providing a convenient way to connect together two mounting cases within the same swing frame, or stacked vertically between the same mounting rails.

The cable can be folded for installation convenience and can be flexed indefinitely to a radius as small as several inches.

Cable impedance is 100 ohms, allowing direct connection between J Series logic circuits up to 115 inches apart, without the necessity of going through cable driver/receiver circuits.

Now the user can wire and test mounting cases individually, then interconnect with ribbon cable. This eliminates the need to run logic wire across several adjacent backplanes.



ZT46 Ribbon Cable

WIRING COMPONENTS AND TOOLS

ZT52 Logic Wire

The wire required for connection to back panel wrap terminals is a special type, with high tensile strength solid copper wire and a cut-proof insulation. The usual insulation, made from polyethylene or teflon, tends to cold flow over a period of time when placed under pressure such as exists when a wire is pulled tight against a wrap post. Eventually this causes intermittent short circuits which are extremely hard to find. SDS provides a 1,000 foot spool of wire, Model ZT52, for making wrapped connections. The same wire is suitable for soldered connections although a softer copper can be used since the wire need not grip the post.

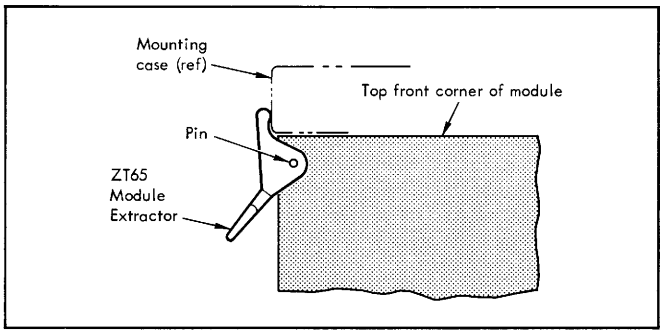
VT10 Jumper Kit

Model VT10 jumper kit contains an assortment of 500 slide-on jumper wires, primarily for use in systems whose wiring requires frequent change. This new approach offers significant improvements in reliability and convenience over taper pin techniques. The terminals at the ends of each wire slide on wire-wrap pins. Terminals may be stacked two high on each pin. Wire is No. 24 AWG insulated stranded copper. Wire lengths within each kit are:

Length	Quantity	Length	Quantity
1.0"	80	8.0"	20
2.0"	80	10.0"	20
3.0"	80	12.0"	15
4.0"	80	15.0"	10
5.0"	60	18.0"	10
6.5"	40	27.0"	5

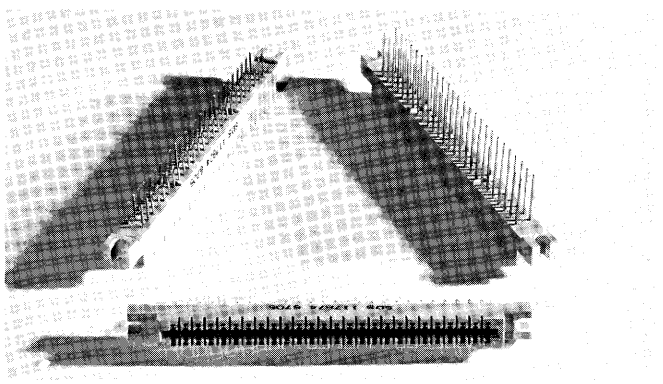
ZT65 Module Extractor

The ZT65 is a small plastic lever that mounts on any SDS module. It provides the mechanical leverage and bearing surface needed to make module removal simple and convenient.



VT11 and VT12 Back-panel Connectors

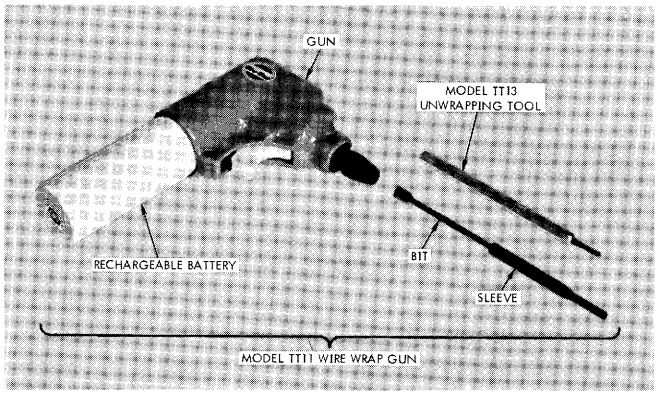
Model VT11 Connector with wire-wrap pins and Model VT12 Connector with solder-tails are provided for special module installations. They are identical to those used in the MT mounting cases.



VT12 (Solder-tail) and VT11 (Wire-wrap) Connectors

TT11 and TT13 Wire Wrapping Tools

The Model TT11 Cordless Power Wire Wrap Gun, with bit, sleeve, and rechargeable battery is offered, as is the Model TT13 hand-operated unwrapping tool, needed to remove improper wraps.



Models TT11 and TT13 Wire Wrapping Tools

SERVICES

SDS has found that its customers build systems in less time and at lower cost when a number of services are readily available.

APPLICATION ENGINEERING

Application Engineers and technically oriented Sales Engineers are available at regional offices to aid in specifications writing, system planning, and preliminary logic design. These SDS digital engineers have considerable experience in the design of both small and large scale digital and analog systems. Typical recent applications include: specialized data processors to compensate for earth curvature, telemetry data converters, missile test sequencers, a digital phase meter, a digital control for a large data display, typesetting machine controllers, industrial process controls, data reduction from linear accelerators, medical research data processors, and interfacing units for SDS Sigma Computers.

FABRICATION INSTRUCTIONS

An application bulletin is provided, SDS Pub. No. 64-51-07, which describes in detail the procedures used during final assembly and wiring of a J Series or T Series system. It gives complete, step-by-step illustrated instructions including part numbers and names of supplies for all tools and supplies needed.

SPECIAL MODULE DESIGN

The SDS Engineering Department will design and build modules with special configurations of standard J Series circuits, to customer specifications. Sometimes this approach leads to lower total cost, particularly when a large number of similar modules are required.

AUTOMATED WIRE LISTING (AWL)

A computerized wire listing service is now available, to save engineering time and greatly improve the design of backplane wiring. The user submits his logic design on forms furnished by SDS. Upon completion of the data processing cycle he receives a wiring book which lists all wires in order of installation. The optimum wire lengths, routing, and nesting patterns are calculated by the computer program, and the results are incorporated in the wire list. For detailed information about this service request SDS Publication No. 64-51-11.

AUTOMATED WIRING SERVICE (AWS)

For those users who do not have the facilities to conveniently wire mounting cases, and for those who wish additional wiring capability, SDS now offers an automated wiring service. Any J Series chassis will be wired accurately to customer supplied wire lists. Two different listings are required: a list of wires with two columns, each column representing one end of each wire (a From-Pin column and a To-Pin column); and a pin count list which shows how many wires are connected to each pin on each connector. For best performance SDS recommends that the wire lists be prepared by SDS Automated Wire Listing.

Significant cost savings and increased reliability result from the application of automated wire-wrap equipment to the manufacture of backplanes. For additional information, request SDS Publication 64-51-12.

WARRANTY

SDS offers a standard one year warranty on all equipment.

REFERENCES

Detailed descriptions of cabinets, mounting cases, power supplies, and cabling are given in SDS publication 64-51-15. Other publications mentioned in this catalog are:

1. Assembly and Wiring, 64-51-07
2. Automated Wire Listing, 64-51-11
3. Automated Wiring Service, 64-51-12.

J SERIES PRODUCT INDEX AND PRICE LIST

Effective Date: 15 December 1968

QUANTITY DISCOUNTS

Order Exceeding	Discount	Order Exceeding	Discount
$ 5,000	3%	$ 50,000	10%
10,000	5%	100,000	13%
20,000	7%	200,000	16%
		500,000	20%

Discounts apply to single purchase orders placed and not subsequently altered in any manner by one customer specifying delivery and billing to single addresses.

SDS System Products Department
701 South Aviation Boulevard
El Segundo, California 90245

Model	Page	Description	No. Ckts.	Price
AJ10	20	Cable receivers	14	$150
AJ11	20	Cable receivers/drivers	14	200
AJ12	20	Cable drivers	14	100
AT22	23	Schmitt triggers	2	100
AT69	24	Differential receivers	9	120
BJ10	26	BCD/10-line decoder and lamp driver	1	75
BJ11	28	Binary/16-line decoder	1	60
BJ12	30	BCD/10-line decoders, 3 decades	3	105
BJ60	32	BCD/10-line decoder and lamp driver	1	80
BJ61	34	Binary/16-line decoder	1	65
BJ62	36	BCD/10-line decoders, 3 decades	3	110
CJ16	38	Medium freq. clock oscillator (7.8KHz to 2MHz)	1	125 ⓒ
CT10	39	High freq. clock oscillator (1MHz to 10MHz)	1	80 ⓐ
DJ24	40	10-bit D-to-A converter	1	150
ET10-XX	116	14-conductor 33-ohm cable w/connector each end		40 ⓑ
ET11	116	Front-edge cable connectors		7
ET12-XX	116	14-conductor cable		2/ftⓒ
ET13	116	Cable dummy loads, 33 ohms		20 ⓓ
ET14-XX-Y	116	14-conductor 33-ohm cable w/connector one end		30 ⓔ
ET24	117	BNC connector tray		65
FJ10	41	J-K flip-flops	8	56

ⓐ Add $25 for each crystal. Specify frequency.
ⓑ $40 for basic assembly + $2 per foot of cable up to 50 feet. XX denotes cable length in feet. Order ET13 or ET11 for each end of cable that is not "chained" in both directions.
ⓒ $2 per foot of cable up to 50 feet.
ⓓ Order dummy load for end of cable.

Model	Page	Description	No. Ckts.	Price
FJ11	42	4-bit binary bidirectional counter-register	1	$ 70
FJ12	45	Universal flip-flops	5	50
FJ13	46	4-bit storage registers	4	88
FJ14	48	8-bit shift registers	2	120
FJ16	50	BCD counter/decoder and 10-line lamp driver	1	90
FJ17	52	Binary counter/16-line decoder	1	95
FJ18	54	BCD bidirectional counter, 3 decades	3	175
FJ19	56	8-bit storage registers	2	65
FJ20	56	10-bit storage registers	2	75
FJ21	56	12-bit storage registers	2	96
FJ60	58	J-K flip-flops	8	65
FJ61	59	4-bit binary bidirectional counter-register	1	75
FJ62	61	Universal flip-flops	5	55
FJ63	62	4-bit storage registers	4	95
FJ64	64	8-bit shift register	2	125
FJ66	66	BCD counter/decoder and 10-line lamp driver	1	100
FJ67	68	Binary counter/16-line decoder	1	100
FJ68	70	BCD bidirectional counter, 3 decades	3	180
HT58	72	Universal operational amplifier	1	170
HT72	74	General purpose operational amplifiers	2	79
HT73	75	Voltage comparators	9	120

ⓔ $30 for basic assembly + $2 per foot of cable up to 50 feet. XX denotes cable length in feet. Specify Y as C or E for connector mounting on Component or Etch side of module. Order ET13 or ET11 for each end of cable that is not "chained" in both directions.

Prices and specifications are subject to change without notice.

Model	Page	Description	No. Ckts.	Price
IJ10	77	2-input NANDs (14), inverters (2)	16	$ 40
IJ11	78	3-input NANDs (4), 4-input NANDs (6)	10	50
IJ12	79	2-input NANDs (6), inverters (14)	20	48
IJ13	80	2-in power NANDs (passive external pull-ups)	18	60
IJ14	81	2-in power NANDs (DTL with active pull-ups)	18	60
IJ16	82	4-in power NANDs (DTL with active pull-ups)	10	50
IJ60	83	2-in NANDs (14); inverters (2)	16	45
IJ61	84	3-in NANDs (4); 4-in NANDs (6)	10	50
IJ62	85	2-in NANDs (6); inverters (14)	20	55
IJ64	86	2-in power NANDs (TTL with active pull-ups)	18	66
IJ66	87	4-in power NANDs (TTL with active pull-ups)	10	55
LJ11	88	4 x 8 transfer gate (digital multiplexer)	1	69
LJ12	89	AND-ORs/Exclusive-ORs (7); driver (1)	8	58
LJ16	90	4-bit parallel binary adder	1	75
LJ17	93	8-input NANDs	5	50
LJ61	94	4 x 8 transfer gate (digital multiplexer)	1	75
LJ62	95	AND-ORs/Exclusive-ORs (7); driver (1)	8	65
LJ66	96	4-bit parallel binary adder	1	80
MT10	115	Fixed mount case, solder-tail pins		220
MT12	115	Fixed mount case, wire-wrap pins		150
MT13	115	Fixed mount case without backplane		30
MT30	115	Hinged mount case, solder-tail pins		240
MT32	115	Hinged mount case, wire-wrap pins		160
MT33	115	Hinged mount case without backplane		40
MT42	115	Two-high/one-high combination fixed mount case		300
MTD-1	115	Drawer type 90-module case, solder-tail pins		700
MTD-2	115	Drawer type 90-module case, wire-wrap pins		700
NT18	99	Negative logic to SDS interface gates	8	55
NT33	100	SDS to negative logic interface gates	8	55
OJ14	101	Medium-delay one-shots (50 μsec. to 2.2 sec.)	4	160
OJ18	102	Adjustable one-shots (100 nsec. to 20 μsec.)	4	140
PT10	116	Compact power supply		280
PT23	116	Digital and analog (50v, 25v) supply		830
PT24	116	Digital and analog (25v) supply		830
PT26	116	Analog (50v, 15v) supply		180
QJ17	103	Indicator lamps, 4-input gated	12	100
RJ10	104	Lamp and relay drivers, gated	8	80
ST14	105	Manually-operated SPDT toggle switches	15	120
TT11	119	Cordless power wire-wrap gun		130
TT13	119	Manual wire-unwrapping tool		15

Model	Page	Description	No. Ckts.	Price
VT10	118	Jumper kit (500 wires)		$125
VT11	118	Individual module connector, wire-wrap pins		5
VT12	118	Individual module connector, solder-tail pins		5
WT49	106	±35 volt reference voltage regulators	2	190
WT53	107	±25 volt reference voltage regulators	2	80
WT54	107	±15 volt reference voltage regulators	2	80
XJ10	108	Individual 1.1K ohm pull-up resistors	46	34
XJ11	109	Test lamp assembly	10	95
XJ12	110	MSI module		18
XJ13	110	MSI module (for TI packages)		18
YT14	114	24-inch cabinet		750
YT19	114	19-inch system cabinet		1200
YT24	114	24-inch system cabinet		900
YT30	114	Side panel		100
YT31	114	Front door, no cut-out		170
YT32	114	Front door with cut-out and control panel		400
YT43	114	3-high swing frame		500
YT47	114	7-high swing frame		650
YT49	114	9-high swing frame		700
ZJ10	110	Socket module	32	95
ZJ12	110	Breadboard module (dual-in-lines only)		18
ZJ14	111	2-high socket module	64	190
ZT11	111	Blank module		20
ZT15	112	Cable-plug module (solder connections)		30
ZT17	116	19-inch hinged door, 5-1/4 inches high		40
ZT18	116	19-inch hinged door, 10-1/2 inches high		50
ZT19	116	19-inch hinged door, 15-3/4 inches high		60
ZT20	116	Blower assembly		80
ZT23	112	Cable-plug module (front-edge clamp)		25
ZT37	113	Breadboard module (dual-in-line and TO-5)		20
ZT40-1	116	Push-on panel, 1-3/4 inches		35
ZT40-2	116	Push-on panel, 3-1/2 inches		35
ZT40-3	116	Push-on panel, 5-1/4 inches		35
ZT40-4	116	Push-on panel, 7 inches		45
ZT45	117	Ribbon cable with connectors, vertical		100
ZT46	117	Ribbon cable with connectors, horizontal		100
ZT52	118	Backpanel wire, 1,000 ft. spool No. 28 AWG		60
ZT53	113	Extender module		40
ZT60	113	Copper-clad blank module		20
ZT65	118	Module extractor (package of 32)	32	25

SDS

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